Low-Voltage Wide-Band NMOS-Based Current Differencing Buffered Amplifier

W. Tangsrirat¹, Member, K. Klahan¹, K. Kaewdang¹, Non-members, and W. Surakampontorn¹, Member

¹Faculty of Engineering, King Mongkut’s Institute of Technology Ladkrabang, Ladkrabang, Bangkok 10520, Thailand
E-mail : ktworapo@kmitl.ac.th , kswanlop@kmitl.ac.th

ABSTRACT
An integratable circuit technique to realize a low-voltage current differencing buffered amplifier (CDBA) is introduced. The realization scheme is through the modification of a low-input resistance CCII+ and the proposed CDBA can operate with the minimum supply voltage of ±1.25V. In order that the signal path consists of only NMOS transistors, a negative current mirror using NMOS transistors is employed. With standard 0.5-µm CMOS process parameters, PSPICE simulation results show that the proposed CDBA provides the terminal resistances of \( r_n = r_p = 32\, \Omega \), \( r_z = 144k\, \Omega \), \( r_w = 9\, \Omega \), and the -3dB bandwidth of about 400 MHz. An universal CDBA-based filter is also proposed to demonstrate the usefulness of the CDBA

Keywords: current differencing buffered amplifier (CDBA), CMOS transistor, current-mode circuit.

1. INTRODUCTION

Recently, an active circuit element called as a current differencing buffered amplifier (CDBA) has been introduced [1]. The CDBA provides the advantages, particularly in the realization of continuous-time filters, in that it simplifies the implementation, being free from parasitic capacitances, quite suitable for current mode operation and can operate in the frequency range of more than tens of MHz [1]-[3]. The CDBA is also useful for oscillator design [4]. To realize the CDBA, two commercially available current feedback amplifiers (CFAs), AD844, can usually be used, where the CFAs are formed as second generation current conveyors (CCIIIs) and voltage buffers [1,4]. However, the CDBA characteristic is dominated by the property of the CFA. Recently, a CDBA in integrated circuit form has been proposed, but it is only suitable for implemented in bipolar technology [3]. For CMOS technology, so far there are two implementation schemes that have been reported in the literatures [2,5]. However, the terminal resistances of the CMOS based CDBA are quite high, in the order of several hundred ohms, and its voltage gain is much less than one, i.e., \( \approx 0.7 \). Thus, the application of the CDBAs is limited and, in practical application, methods to compensate these effects should be included [6]. In addition, most of the existed CDBAs are operated at high supply voltages. The advance in integrated circuit technology makes the devices in an IC form so small and the power supply voltage of the circuits must restricted to a low value. Furthermore, with the increasing demands for battery-operated portable equipments, single battery operation equipment is now most essential. Thus, a CDBA with very low input terminal resistances and can be operated in low supply voltage operation is more preferable.

Usually, a current differencing function can be achieved through negative current mirror using PMOS transistors. For a typical n-well CMOS process, the unity gain frequency \( f_t \) of NMOS device is approximately two times higher than the \( f_t \) of PMOS devices, due to electrons have a higher saturation velocity compared to holes [7]. In addition, to realize the same transconductance with transistors of the same gate length, a PMOS gate length must be 3 times wider than a NMOS. This is because the junction capacitance per unit area is approximately 2 times larger for PMOS than for NMOS [8]. Therefore, in order to avoid the limitation of the high frequency operation effecting from PMOS transistors, the CDBA should be designed so that signals pass through only NMOS transistors.

The major goal of this paper is to propose a simple low-voltage NMOS-based CDBA, which has a low resistance at both the current-input terminals (p, n) and at the output-voltage terminal (w). The realization method is based on the modification of a low impedance current conveyor (CCII+) to function as a current differencing circuit and a voltage buffer circuit [9]. To achieve a maximum high frequency response, the CDBA is designed such that the signal has an all NMOS signal path, where a negative current mirror using only NMOS transistors is proposed. Moreover, three-input and single-output current-mode universal biquadratic filter using CD-
BAs is also presented. The proposed filter can realize simultaneously the highpass (HP), lowpass (LP), bandpass (BP), bandstop (BS) and allpass (AP) responses without changing the circuit configuration. The natural angular frequency $\omega_0$ and the quality factor $Q$ are independently controllable through the passive elements, and have low passive and active sensitivities. The performances of the filter using the proposed CDBA are also included.

2. CIRCUIT CONFIGURATION

2.1 Basic concept

From the circuit symbol of the Fig.1, a CDBA is a four terminal analog building block described by the following relations [1]:

$$
\begin{bmatrix}
  i_z \\
  v_w \\
  i_p \\
  i_n \\
\end{bmatrix} =
\begin{bmatrix}
  0 & 0 & 1 & -1 \\
  1 & 0 & 0 & 0 \\
  1 & 0 & 0 & 0 \\
  1 & 0 & 0 & 0 \\
\end{bmatrix}
\begin{bmatrix}
  v_z \\
  i_w \\
  i_p \\
  i_n \\
\end{bmatrix}
$$

(1)

The CDBA can be considered as a transimpedance amplifier that converts the difference of the input currents $i_p$ and $i_n$ at the terminals $p$ and $n$, respectively, into the output voltage $v_w$ at the terminal $w$ through an impedance connected at the terminal $z$. It can be further inferred that the terminal impedances of the $p$ and $n$ terminals must be very low. From the above equation, this device can be realized by a cascade connection of a current differencing and a voltage follower circuits.

2.2 Current differencing circuit

Fig.2 shows the NMOS circuit with a low-input impedance terminal [10]. From the elementary small-signal circuit analysis, the input resistance of this configuration can be calculated as :

$$
r_{in} = \left( \frac{1}{g_{m1}} \right) \left( \frac{1}{1 + F} \right)
$$

(2)

where $F = \left( \frac{g_{m2}g_{m4}r_oB}{g_{m3} + g_{m3}} \right)$, and $g_{mi}$ represents the transconductance of the transistors $M_i (i = 1, 2, 3, 4)$ and $r_oB$ denotes the output resistance of the current source $I_B$. Usually $r_oB >> 1/g_{m1}$, then $F >> 1$. Therefore, the input resistance of this circuit is very low.

Based on the use of the low-input resistance input stage of Fig.2, the unity gain current amplifier can be shown in Fig.3. The biasing circuit, that comprising the transistor $M_6$ and the current source $I_B$, is used to bias the input terminal at ground potential. From routine circuit analysis, the output current $i_{out}$ of this circuit can be expressed as :

$$
i_{out} = - \left( \frac{F}{1 + F} \right) i_{in}
$$

(3)

where usually $F >> 1$ then the output current $i_{out}$ can be approximated to :

$$
i_{out} \cong -i_{in}
$$

(4)

Normally, two of the unity-gain current amplifier circuits can be used to accept the input currents $i_p$ and $i_n$. Then, the differential current between $i_p$ and $i_n$ (or $i_p-i_n$) can be achieved by a negative current mirror, formed by PMOS transistors, as shown in
Fig. 4: (a) conventional negative current mirror (b) proposed NMOS-based negative current mirror

Fig. 5: Proposed NMOS-based current differencing circuit

Fig. 6: Buffered voltage amplifier

Fig. 4(a). As the reasons mentioned previously, the negative current mirror would be the major high frequency limitation. To increase the circuit bandwidth, an unity-gain NMOS-based negative current mirror shown in Fig 4(b) is proposed, where M7-M10 form as a positive current mirror. Since the NMOS transistors provide the basic current mirror action, thus its performance is equivalent to NMOS positive current mirror. Note that the voltage at point A must be high such that all devices are in the on state. If we assume that all transistors are well matched, then an output current $i_{out}$ of this circuit is approximately equal to an input current $i_{in}$ (or $i_{out} \approx i_{in}$).

Fig. 5 shows the proposed NMOS-based current differencing circuit. The current source $I_B$ and transistors $M_0$ are used to bias the terminals $p$ and $n$ at ground potential. Groups of transistor (M1-M5) and (M1-M5) form two unity-gain current amplifiers that produce the currents ($I_B - i_p$) and ($I_B - i_n$) at the drains of M5 and M5, respectively. Due to the negative current mirror M7-M10, the drain current of M8 is equal to ($I_B + i_n$). Therefore, the signal current $i_z$ of the terminal $z$ can be expressed as

$$i_z = 2I_B - [(I_B - i_p) + (I_B + i_n)] = i_p - i_n. \quad (5)$$

In order to account for the non-ideal performance, let $\alpha_p$ and $\alpha_n$ are the current gains for the inputs from the terminals $p$ and $n$, respectively. From routine circuit analysis, the output current $i_z$ can be given
2.3 Buffered voltage amplifier

The buffered voltage amplifier, where the transistor \( M_{11} \) and the two bias current sources \( I_B \) are connected as voltage level shift. The relationship of the voltages at the terminals \( w \) and \( z \) (or \( v_w \) and \( v_z \)) can be expressed by:

\[
v_w = \beta_v \cdot v_z
\]

(9)

where

\[
\beta_v = \left( \frac{g_{m11}r_{oB}}{1 + g_{m11}r_{oB}} \right) \left[ \frac{g_{m12} \left( 1 + \frac{g_{m15}r_{oB}}{2} \right)}{g_w + g_{m12} \left( 1 + \frac{g_{m15}r_{oB}}{2} \right)} \right],
\]

\( g_w = 1/R_w \) and \( R_w \) is the resistor connected at the terminal \( w \). If \( g_{m11}r_{oB} \gg 1 \) and \( g_{m12} \left( 1 + \frac{g_{m15}r_{oB}}{2} \right) \), then \( v_w \approx v_z \). Similar to the equation (2), since \( M_{12} \) and \( M_{15} \) are connected as a low-input resistance input stage, the output resistance of the terminal \( w \) becomes quite low and is equal to

\[
r_w = \left( \frac{1}{g_{m12}} \right) \left( \frac{1}{1 + F_w} \right)
\]

(10)

where

\[
F_w = \left( \frac{g_{m13}g_{m15}r_{oB}}{g_{m13} + g_{m14}} \right).
\]

If \( r_{oB} \gg 1/g_{m11} \), the input resistance looking into the terminal \( z \) becomes a high value and is approximated to

\[
r_z = \frac{r_{oB}}{2}
\]

(11)

2.4 Proposed low-voltage wide-band NMOS-based CDBA

Fig.7 shows the proposed low-voltage NMOS-based CDBA, which is based on the use of the proposed current differencing (\( M_1-M_{10}, M_1-M_5 \)), and the buffered voltage amplifier (\( M_{11}-M_{15} \)) circuits. From the circuit diagram, it can be considered from the positive to the negative supply voltages that the proposed circuit uses only two NMOS transistors and one PMOS transistor (or one bias current source). Therefore, the circuit can operate at a low power supply voltage of \( (2V_{DS1} + V_{IB}) \), where \( V_{DS1} \) and \( V_{IB} \) are the drain-to-source voltage of the transistor \( M_i \) and the voltage drop at the bias current source \( I_B \), respectively. As an example, for the standard 0.5-\( \mu \)m CMOS process parameters, the threshold voltages \( V_{TN} \) and \( -V_{TP} \) of the NMOS and PMOS transistors
are about 0.64V and 0.91V, respectively. If the bias current sources $I_B$ are realized by the basic current mirrors, as a result, the minimum supply voltage is about $[2(0.64V)+(0.91V)] = 2.19V$ or ±1.095V.

**Fig.8:** dc transfer characteristics of the CDBA
(a) current transfer characteristics
(b) voltage transfer characteristic

3. SIMULATION RESULTS AND APPLICATION

3.1 Proposed CDBA characteristics

The characteristics of the proposed CDBA of Fig.7 have been studied through PSPICE using the 0.5-$\mu$m CMOS LEVEL3 SCN05H technology supplied by MOSIS (vendor: HP-NID) [10]. The aspect ratios of the transistors used are as follows: $W/L = 20$ for the NMOS $M_1$-$M_5$, $M_1$-$M_5$, and $W/L = 40$ for the NMOS $M_7$-$M_{15}$. The supply voltages used are $V_{DD} = -V_{SS} = 1.25V$, and the bias currents are $I_B = 30\mu$A. Grounded resistors $R_z = 1$ kΩ and $R_w = 10$ kΩ are connected at the terminals $z$ and $w$, respectively.

Fig.8 shows the dc transfer characteristics of the output current $i_z = i_p - i_n$ against the input current $i_n$, Fig.8(a), and the output voltage $v_w$ against $v_z$, for different values of the input current $i_p$, Fig.8(b). It is evident that the CDBA can convert the differential input current into the output voltage with high accuracy and linearity over the entire dynamic range ($I_B = 30\mu$A). From Fig.8(a), the maximum offset currents from the terminals $p$ and $n$ to the terminal $z$ is equal to 1.2μA, which is mainly due to the influence of the current transfer errors from the mismatched mirroring transistors. In Fig.8(b), the offset voltage from terminals $z$ to $w$ appears to be about 3.5mV, owing to mismatch in the current scale factor between $M_{11}$ and $M_{12}$. From the simulation, it is found from that deviation from its ideal curve is less than 12% within the range -100mV to +100mV. Also from the simulations, the circuit power consumption for $i_p = i_n = 0$ is 0.98mW and for $i_p = i_n = 30\mu$A is 1.22mW, and the resistances of the terminals $p$, $n$, and $w$ ($r_p$, $r_n$, $r_z$ and $r_w$) are equal to $32\Omega$, $32\Omega$, 144kΩ and 9Ω, respectively.

Fig.9 shows the ac transfer characteristics of the proposed CDBA. The current and voltage gains $\alpha_p, \alpha_n$, and $\beta v$ are found to be 0.992, 0.983 and 0.991, which corresponding to the errors of 0.8%, 1.7% and 0.9%, respectively. The -3dB bandwidths of the current gains $i_z/i_p$ and $i_z/i_n$, and the voltage gain $v_w/v_z$, are respectively located at 628MHz, 642MHz and 432MHz. As shown in the figures, the proposed realization leads to high accuracy and high frequency operation, which is excellent over a high frequency range extending beyond 432MHz. Note that the major high-frequency limitation of the circuit is due to
the pole \( P_w \) at the terminal \( w \), which is directly proportional to \( R_w \) and can be given by

\[
P_w \approx - \left[ g_{m12} R_w \frac{1 + g_{m12} R_w}{2} \right] \left[ \frac{1 + g_{m12} R_w}{2} \right] \text{(12)}
\]

where \( g_{m13} \) is the gate-to-source capacitance of the transistor \( M_{13} \). This pole frequency can be extended by increasing the value of \( R_w \), for example, for \( R_w = 20 \, \text{kΩ} \), the pole frequency \( P_w \) is located at 510 MHz.

### 3.2 Current-mode biquadratic filter using CDBAs

In this section, an universal current-mode multifunction biquadratic filter as shown in Fig. 10 has been proposed. From routine circuit analysis, the current transfer function is as follows.

\[
I_{out} = s^2 \left( 1 + \frac{1}{s R_5 C_2} I_{in3} \right) - s \left( \frac{1}{R_5 C_2} \right) I_{in2} + \left( \frac{1}{R_1 R_5 C_3 C_2} I_{in1} \right)/D(s) \text{(13)}
\]

where

\[
D(s) = s^2 + s \left( \frac{1}{R_5 C_2} \right) + \left( \frac{R_3}{R_1 R_5 R_4 C_3 C_2} \right).
\]

The parameters \( \omega_0 \) and \( Q \) of the filter can be expressed as:

\[
\omega_0 = \sqrt{\frac{R_3}{R_1 R_2 R_4 C_1 C_2}} \text{(14)}
\]

and

\[
Q = R_5 \sqrt{\frac{R_3 C_2}{R_1 R_2 R_4 C_4}} \text{(15)}
\]

The sensitivities with respect to the circuit passive parameters can be written as:

\[
S_{\omega_0}^{\omega_0} = \frac{1}{R_3} \frac{\partial \omega_0}{\partial R_3} = -\frac{1}{2} \text{(16)}
\]

\[
S_{R_5}^{\omega_0} = 0 \text{(17)}
\]

\[
S_{R_1,R_2,R_4,C_1,C_2}^{\omega_0} = -\frac{S_{R_3}^{\omega_0}}{2} = -\frac{1}{2} \text{(18)}
\]

\[
S_{R_5}^{\omega_0} = 1 \text{(19)}
\]

All the filter passive sensitivities are within unity in magnitude. Furthermore, if setting \( R_1(j = 1, 2, \ldots, 4) = R \) and \( C_1 = C_2 = C \), then the circuit parameters \( \omega_0 \) and \( Q \)-factor can be rewritten as:

\[
\omega_0 = \frac{1}{RC} \text{(20)}
\]

and

\[
Q = \frac{R_5}{R} \text{(21)}
\]

It is interesting to note that the \( Q \)-factor parameter can independently be controlled by adjusting \( R_5/R \) without taking an effect to the \( \omega_0 \), which is adjusted by \( R \) and/or \( C \). Moreover, the highpass (HP), lowpass (LP), bandpass (BP), bandstop (BS) and allpass (AP) output currents will be obtained by selecting input currents appropriately from these specifications:

1. HP filter where \( I_{in2} = I_{in3} \) are input currents and \( I_{in1} = 0 \).
2. LP filter where \( I_{in1} \) is an input current and \( I_{in2} = I_{in3} \).
3. BP filter where \( I_{in2} \) is an input current and \( I_{in1} = I_{in3} \).
4. BS filter where \( I_{in1} = I_{in2} = I_{in3} \) are input currents and \( R_5 = R \).
5. AP filter where \( I_{in1} = I_{in2} = I_{in3} \) are input currents and \( R_5 = 2R \).

By taking into consideration the non-idealities of the CDBA on the frequency performance, the current-voltage relations in equation (1) can be expressed as:

\[
i_{z1} = \alpha_{pi1}i_P - \alpha_{ni}i_n \text{ and } v_{w1} = \beta_1v_z, \quad i_{p1} = 1 - \epsilon_{p1}(|\epsilon_{p1}| << 1), \quad \alpha_{ni} = 1 - \alpha_{ni}(|\epsilon_{ni}| << 1), \quad \beta_1 = 1 - \epsilon_{v1}(|\epsilon_{v1}| << 1), \quad \text{and} \quad \epsilon_{p1} \text{ and } \epsilon_{v1} \text{ are the current tracking errors from the terminal } p \text{ and from the terminal } n \text{ to the terminal } z \text{, and } \epsilon_{v1} \text{ is the voltage tracking error from the terminal } z \text{ to the terminal } w \text{ of the } i\text{-th CDBA, respectively. In this case, reanalysis the proposed filter configuration of Fig.10 yields the non-ideal natural angular frequency } \omega_0 \text{ and quality factor } Q \text{ as:}
\]

\[
\omega_0 = \sqrt{\frac{\alpha_{p1}\alpha_{p2}\alpha_{p3}\alpha_{n1}\beta_1\beta_2}{R_1 R_5 R_4 C_3 C_2}} \text{(22)}
\]

and

\[
Q = \frac{R_5}{\alpha_{n2}} \sqrt{\frac{\alpha_{p1}\alpha_{p2}\alpha_{p3}\alpha_{n1}\beta_1\beta_2 R_4 C_3 C_2}{\beta_2 R_1 R_2 R_4 C_1}} \text{(23)}
\]

For this case, all active sensitivities of the \( \omega_0 \) and \( Q \) with respect to \( \alpha_{ni} \), \( \alpha_{pi} \), and \( \beta_1 \) are less than unity.

Fig.11 shows the simulated frequency responses of the filter using the proposed CDBAs, when \( R_j = 1 \, \text{kΩ} \), excepted in AP case the resistor \( R_3 = 2 \, \text{kΩ} \), and \( C_1 = C_2 = 0.159 \, \text{nF} \). These values are selected to...
obtain $Q$-factor = 1 at a natural frequency $f_0$ ($\omega_0/2\pi$) = 1 MHz. The corresponding $f_0$ for the HP, LP, BP, BS, and AP responses measured from the simulations are found to be 0.72 MHz, 1.14 MHz, 0.90 MHz, 0.94 MHz, and 0.91 MHz, which differ from the predicted values of about 28%, 14%, 6.35%, 5.45% and 9.38%, respectively. This confirms that the filter can simultaneously realize all standard filtering functions in the same configuration by properly choosing input currents.

To demonstrate the independent adjustable of the $f_0$ without effecting the $Q$-factor, Fig.12 shows the BP current responses when the $f_0$ is respectively set to 200 kHz, 1 MHz and 5 MHz through changing resistors $R_j$ to 5 kΩ, 1 kΩ, and 200 Ω, respectively, while the $Q$-factor in this case is set to constant at $Q$=1. It should be noted from the simulated results that the various values of the $f_0$ can be adjusted by varying $R_j$ without disturbing the $Q$-factor.

For the controllability of $Q$-factor by adjusting the ratio of $R_5/R$, the simulated frequency responses of the BP filter, when $Q$-factor is respectively adjusted to 1, 5 and 10 while keeping $f_0$ constant at 1 MHz, are shown in Fig.13. The $Q$-factor that calculated from the simulation response are 1, 4.87 and 11.06, respectively, which are close agreement with the desired value.

4. CONCLUSION

A circuit configuration for realizing low-voltage current differencing buffered amplifier (CDBA) in MOS technology has been described. The proposed circuit can be operated at low power supply voltage (±1.25V) and can easily be implemented in monolithic integrated circuit. The simulated responses with PSPICE have been quite good over the frequency range of about 400MHz, with low-power consumption. Owing to the dominant pole $P_{e}$, the improvement of the frequency performance of the buffered voltage amplifier is our further investigated. We also demonstrate that a current-mode universal biquadratic filter using the proposed CDBA as active elements provides the response close to the theoretical prediction.

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References


Worapong Tangsrirat received the B.Ind.Tech. degree (Honors) in Electronics, the M.Eng., and the D.Eng. degrees in Electrical Engineering from the King Mongkut’s Institute of Technology Ladkrabang (KMITL), Bangkok, Thailand, in 1991, 1997 and 2003, respectively. He has joined the Faculty of Engineering, KMITL as a faculty member since 1995, and is presently an assistant professor in the Department of Control Engineering. His research interests are mainly in analog integrated circuits and active filter design. He is a member of the ECTI and the IEEE.

Katesuda Klahan was born in 1977. She received B.Eng. degree in Electrical Engineering from Ubonratchathani University and M.Eng. degree in Electronics from King Mongkut’s Institute of Technology Ladkrabang (KMITL), in 1999 and 2002 respectively. Now she is a doctoral degree student in Electrical Engineering at the KMITL. Her research area is Analog Integrated Circuit Design and Analog Signal Processing.

Khanittha Kaewdang received the B.Eng. degree in Electrical Engineering from Ubonratchathani University, Ubonratchathani, Thailand, in 1999 and the M.Eng. degree in Electronics from the King Mongkut’s Institute of Technology Ladkrabang (KMITL), Bangkok, Thailand, in 2002. Currently, she is a doctoral degree student in Electrical Engineering at the KMITL. Her research interests are in the field of Analog Integrated Circuit Design.

Wanlop Surakampontorn received the B.Eng. and M.Eng. degrees in Electrical Engineering from the King Mongkut’s Institute of Technology Ladkrabang (KMITL), Bangkok, Thailand, in 1976, and 1978, respectively, and the Ph.D. in Electronics from the University of Kent at Canterbury, Kent, U.K., in 1983. Since 1978, he has been a member of the Department of Electronics, Faculty of Engineering, KMITL, where he is currently a Senior Professor of Electronic Engineering. His research interests are in the areas of analog and digital integrated circuit designs, real-time application of PC computers and microprocessors, digital signal processing, electronic instrumentation, and VLSI signal processing. He is a member of the IEICE of Japan, a senior member of the IEEE and a member of the ECTI.