

Design of 1.8-V CMOS Polyphase Filter for Dual-Mode Bluetooth/ZigBee Transceiver

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ABSTRACT

A dual-mode Bluetooth/ZigBee low-IF polyphase channel filter has been designed with 0.18 μm digital CMOS technology based upon transconductor-capacitor (GmC) structure. The filter has a fifth-order 0.5dB equiripple Chebyshev bandpass response. It achieves a signal-to-noise ratio of 62dB and input referred third-order intermodulation intercept of 33dBVp (for distant blocker interference). The filter consumes a moderate power of 2.5mW from a 1.8-V single supply in both modes of operation.

Keywords: Transconductor, Gm-C, complex filter, Bluetooth, ZigBee.

1. INTRODUCTION

The low-intermediate frequency (low-IF) polyphase architecture has emerged as the preferred approach for achieving the required sensitivity in fully integrated wireless transceivers [1], [2]. Mainly driven by cost and power consumption, standard CMOS solutions for applications such as Bluetooth (IEEE 802.15.1) and ZigBee (IEEE 802.15.4) have set new challenges for circuit designers at both circuit and system levels. Bluetooth system has widely established itself in various well-known applications including wireless headsets, file sharing and printing, while ZigBee (also known as HomeRF Lite) is used for very simple wireless connectivity. The addition of ZigBee capability to a cell phone could enable the control of devices such as lights, electronic devices and central heating using the mobile handset. A dual-mode transceiver solution is being developed because in the price sensitive market for mobile devices, it is essential that this capability be added for minimal extra cost. Noting that coexistence issue of the two standards on the same frequency band is thoroughly discussed in IEEE Standard 802.15.4.

A polyphase filter or complex filter represents one of the key components in low-IF polyphase receiver. Owing to its asymmetric amplitude response, it has

an ability to pass wanted channel signal while efficiently reject neighbouring channel interferers as well as unwanted image. A polyphase filter in this work is based upon transconductor-capacitor structure because of its simplicity, tuneability, linearity and high-frequency performance. The transconductor core circuit follows a linear, wide-tuning, low-noise and compact source degeneration type from [3] where the common-mode feedback and dc gain enhancement has employed a single network according to the topology originally proposed in [4].

2. REVIEW OF COMPLEX FILTERS

Fig.1 shows the basic principle of the complex filter. Starting with a real low-pass filter, the transformation $s \rightarrow s - \omega_0$ is applied. This shifts the poles up the imaginary axis by ω_0 and transforms the lowpass response into an equivalent bandpass response centred at $\omega = \omega_0$. The transformation preserves both amplitude and phase characteristics and produces the required feature of having no image response at negative frequency. Synthesis of complex filters follows similar procedures to those for real filters except that it makes use of complex integrators. Fig.2 shows transformation from real to complex integrators implemented in the G_mC technique. The transfer characteristic of the complex integrator in Fig.2(b) is described by,

$$H(s) = \frac{i_{out}(s)}{i_{in}(s)} = \frac{G}{(s - j\omega_0)C} \quad (1)$$

where ω_0 is frequency shift given by $\omega_0 = G_0/C$. This demonstrates that the transformation $s \rightarrow s - \omega_0$ has been performed as required.

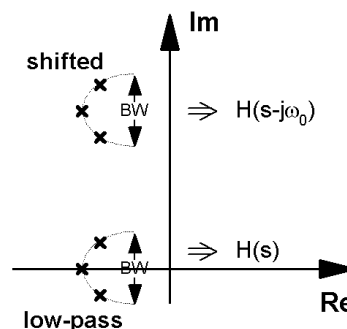


Fig.1: Complex filter basics

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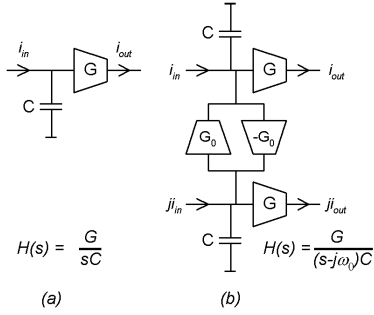


Fig.2: Current-mode G_m - C integrator (a)real (b)complex.

3. TRANSCONDUCTOR CIRCUIT

The variable wide-band resistor source-degeneration transconductor proposed in [3] possesses many advantages including good linearity, low-noise, high frequency capability and low supply voltage. However, such structure inherits a couple of weak points that need special attention. This type of transconductor structure is prone to common-mode instability when employed for filter realisation. It is thus necessary to deploy a common-mode feedback loop comprising common-mode voltage sensing and error amplifiers. Moreover a low dc gain of the transconductor necessitates an additional negative conductance network to provide sufficient dc gain in order to achieve a required filter’s frequency response. As depicted in Fig.3, instead of using two separate networks to enhance common-mode stability and dc gain, a single network (MN3-MN6) adopted from the topology presented in [4] is employed. Its main feature is to ensure common-mode stability where the network forms a low impedance load for common signals and a high impedance load from differential signals, effectively resulting in common-mode stability. The technique has been successfully demonstrated with G_mC filters based on an inverter-type transconductor [5]-[9]. The second important feature is to help increase dc-gain of the transconductor. And this can be simply achieved by sizing transistors so that a positive feedback current from MN5 MN6 is higher than the negative feedback from MN3 MN4. Two-in-one functionality thus allows additional devices to be kept at minimum; hence this helps save extra silicon area and power consumption. The transconductor in Fig.3 possesses a nominal transconductance value of $20\mu S$ ($V_{F3} = 0.7V$). Note that simple cascode PMOS current sources are employed to supply bias currents to the transconductor. The transconductor also deploys a tuning technique from [3]. Five tuning steps are required in this case to ensure a transconductance continuous sweep of $\pm 50\%$ from the nominal value; each tuning voltage can be varied between 0.6V and 1.8V to adjust degeneration NMOS triode resistance. At any time, only one pair of these degeneration

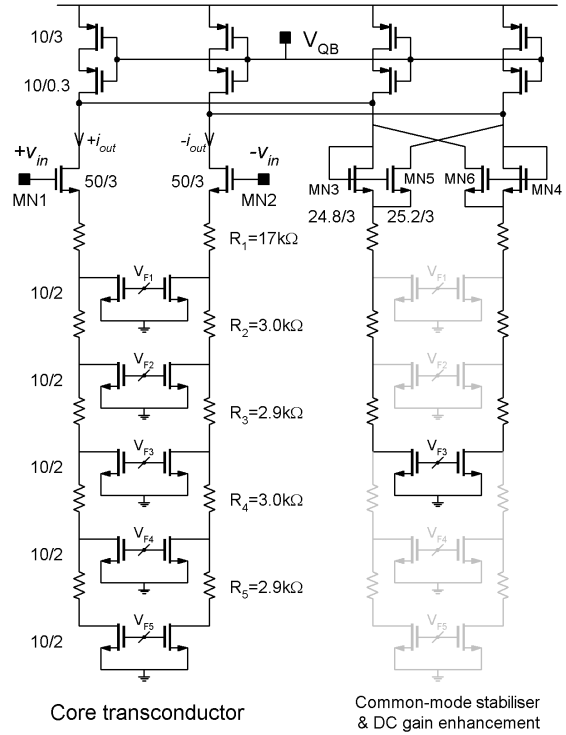


Fig.3: Transconductor with common-mode stabilizer and dc gain enhancement .

NMOS’s is on and the one-side degeneration resistance R_{di} is (only one V_{Fi} is on)

$$R_{di} = \frac{1}{\mu_n C_{ox} (\frac{W}{L})_i (V_{Fi} - V_{th})} + \sum_{n=1}^i R_n \quad (2)$$

μ_n , C_{ox} and V_{th} are conventional parameters for NMOS transistor and the differential transconductance is approximately equal to $1/R_{di}$. To ensure a continuous transconductance sweep, the ladder resistors have to be designed according to (2) so that the adjacent tuning steps have adequate transconductance overlapping at their tuning boundaries when V_{Fi} is switched from one step to another. Because of a limited maximum available tuning voltage of 1.8V, a wide triode resistance variation can be achieved by employing a low threshold voltage NMOS device ($V_{th} = 0.4V$) available in the technology as a tuning triode-MOS resistor. However, it is typical to have large V_{th} for the core transconductor MOS, MN1-MN2. This is because it normally happens that drain and gate voltages swings in opposite directions (sometimes with the same magnitude) from the same quiescent voltage (due to filter’s cascade and feedback structure) and having a large V_{th} device will help maintain the transistors in saturation for large signal swing. Note that some of the transistors and resistors within the common-mode stabiliser (drawn in the light shade) can be omitted to save chip area without severely disturbing the circuit operation. It has only

been included in Fig.3 to imitate the core transconductor structure. Compare this transconductor to the class-AB inverter-type MOS transconductor employed for a dual-mode polyphase filter in [7], [8], [9], the proposed transconductor is inherently insensitive to supply voltage variation and it operates in a class-A manner.

4. FILTER DESIGN

A 5th-order 0.5dB equiripple Chebyshev complex filter depicted in Fig.4 is chosen for this work [7]-[9]. The design values for ZigBee and Bluetooth responses are given in Table I. Notice that the design values are half of those used in [7]-[9] in order to minimise power consumption not higher than 2.5mW (this moderate power consumption has also been achieved by the 5th-order polyphase filter in [10]).

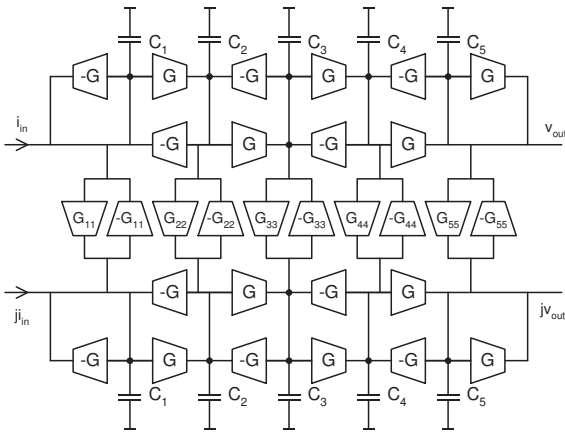


Fig.4: Channel filter architecture.

Table 1: Design values for dual-mode filter

Parameters	Bluetooth	ZigBee
G	20 μ S	20 μ S
G ₁₁	56.86 μ S	56.86 μ S
G ₂₂	41.99 μ S	41.99 μ S
G ₃₃	84.70 μ S	84.70 μ S
G ₄₄	40.99 μ S	40.99 μ S
G ₅₅	56.86 μ S	56.86 μ S
C ₁	9.05 _p F	4.53 _p F
C ₂	6.53 _p F	3.27 _p F
C ₃	13.48 _p F	6.74 _p F
C ₄	6.53 _p F	3.27 _p F
C ₅	9.05 _p F	4.53 _p F

A single feedback loop circuit shown in Fig.5 sets quiescent voltage V_{QB} for all transconductors within the filter. The diode-connected MOS ($W/L = 50\mu m/3\mu m$) emulates the fact that under a quiescent condition, transistors MN3, MN5 and MN4, MN6 within the common-mode reject network in Fig.3 resemble a diode-connected NMOS. In this design the quiescent voltage is set to be at 1V. It should be also

noted that the op-amp employed in Fig.5 is not required to be high performance, hence it can be easily designed under 1.8-V supply.

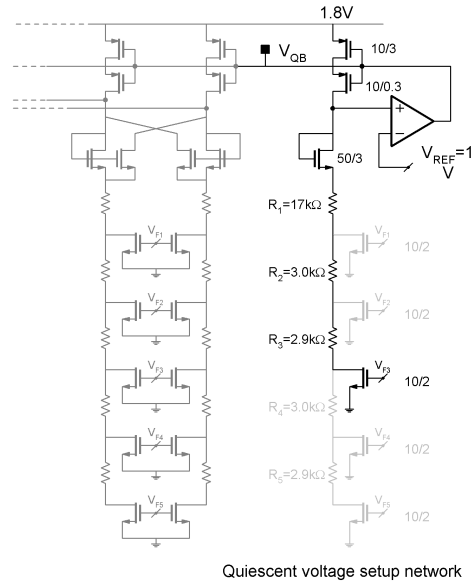


Fig.5: Quiescent voltage setting-up circuitry

5. SIMULATION RESULTS

All the simulations have been carried out using Spectre with Cadence design suite. Simulated frequency response of the complex filter employing 3.3-V 0.18 μ m digital CMOS process is shown in Fig.6-Fig.8. It can be seen that the simulated responses are very close to ideal. Note that the actual capacitor values have been trimmed according to the method described in [8] to take parasitic capacitance into account. Fig.6 shows two modes of operation (Bluetooth and ZigBee), obtained by switching the values of capacitor with the common set of transconductors. Fig.7 illustrates frequency tuning at nominal and two extremes by adjusting tuning voltage. This center frequency tuning capability of $\approx 80\%$ is more than enough to encounter process and temperature variations.

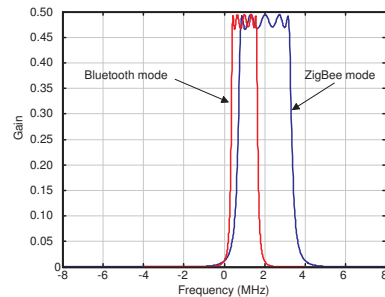


Fig.6: Filter mode switching

The filter common-mode rejection ability has been investigated by measuring common-mode signal fre-

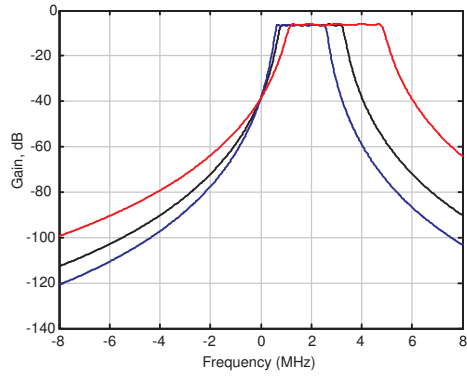


Fig. 7: Frequency tuning in ZigBee mode

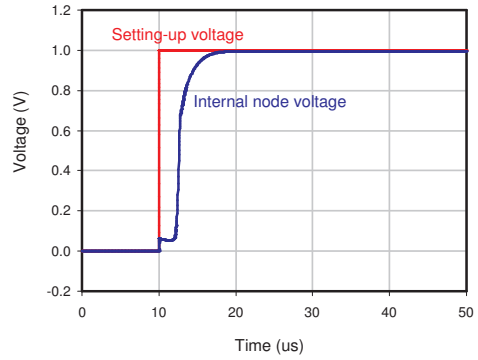


Fig. 10: Stability test with step response

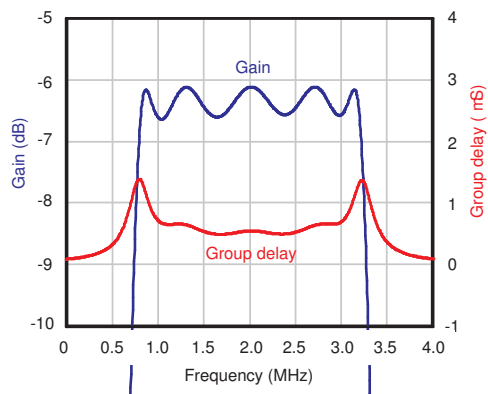


Fig. 8: ZigBee's passband response

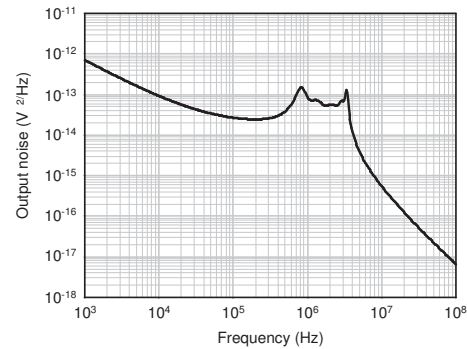


Fig. 11: Noise response (ZigBee mode)

quency response and compare with differential signal as show in Fig.9. It can be seen that although the structure of Fig.3 does not reject common-mode signal locally, but globally the filter does have ability to suppress common-mode signals. The filter has also been subjected to a transient common-mode step response stability test [3], and the results guarantee its unconditional stability as illustrated in Fig.10.

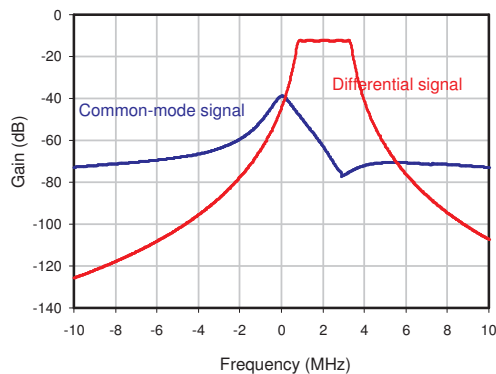


Fig. 9: Filter's frequency response: differential vs common-mode (single-end output)

The ZigBee output differential noise is shown in Fig.11 where the total output noise integrated over the 100MHz bandwidth renders output noise power

voltage of $2.5 \times 10^{-7} V^2$. The ZigBee signal compression characteristic of ZigBee-mode filter is shown in Fig.12 and it demonstrates a linear gain up to an input amplitude of 1Vp (0dBVp) differential and an input referred 1-dB compression point of 1.59Vp (or 4.03dBVp) differential (with corresponding output voltage of 0.68Vp). The signal-to-noise ratio is thus found to be 62.3dB. The in-band spurious free dynamic range (SFDR), where the inter-modulation product has the same power as the filter noise, is found to be 51.3dB and 53.4dB for ZigBee and Blue-

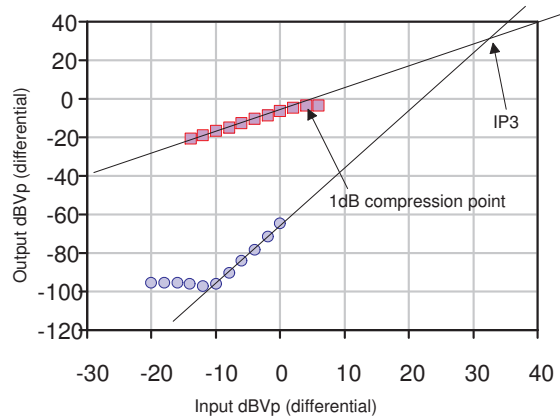


Fig. 12: Third-order intermodulation)

tooth modes respectively. Out-of-band intermodulation of the distant blockers was also simulated as also shown in Fig.12 for ZigBee case (input tones at 6MHz and 10MHz for ZigBee and 3MHz and 5MHz for Bluetooth). It shows the ZigBee third-order intermodulation characteristic indicating an input referred third-order intercept point (IIP3) of 33dBVp differential with corresponding out-of-band SFDR of 59.6dB. The whole filter draws a total current of 1.38mA from a single 1.8-V supply. The overall performance for both modes is summarised in Table 2.

Table 2: Summarised filter performance

Filter Response	Chebyshev	
Filter Order	5+5	
Filter ripple	0.5dB	
Supply voltage	1.8V	
Process	3.3V, 0.18 μ m CMOS	
Supply current	1.38mA	
Mode	Bluetooth	ZigBee
Centre Frequency	1MHz	2MHz
Bandwidth	1.2MHz	2.4MHz
Bandwidth	1.2MHz	2.4MHz
Gain	-6.18dB	-6.18dB
Output noise	$1.4 \times 10^{-7} V^2$	$1.4 \times 10^{-7} V^2$
Input 1dB Comp.	1.59Vp	1.59Vp
Signal/Noise (SNR)	64.9dB	62.3dB
IIP3 (distant blocker)	36.4dBVp	33dBVp
SFDR		
(a) Distant blocker	62.1dB	59.6dB
(b) In-band	53.4dB	51.3dB

6. CONCLUSION

A 1.8V CMOS dual-mode fifth-order polyphase Gm-C filter for Bluetooth/ZigBee transceiver has been designed. The complex bandpass filter is based on Gm-C filter structure with appropriate crossing transconductors to shift lowpass response to the required IF frequencies. It deploys a simple source degeneration transistor integrated with a network, which could simultaneously provide common-mode stability and dc gain enhancement.

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