Realization of Current Controlled Current Differencing Transconductance Amplifier (CCCDTA) and Its Applications

Montree Siripruchyanun and Winai Jaikla, Members

ABSTRACT

This article presents design of a basic current-mode building block for analogue signal processing, named as Current Controlled Current Differencing Transconductance Amplifier (CCCDTA). Its parasitic resistances at two current input ports can be controlled by an input bias current. Owing to working in current-mode of all terminals, it is very suitable to use in a current-mode signal processing, which is continually more popular than a voltage one. The proposed element is realized in a bipolar technology and is examined the performance through PSPICE simulations. They display usability of the new active element, where the maximum bandwidth is 65MHz. The CCCDTA performs low-power consumption and tuning over a wide current range. In addition, some examples as a current-mode universal biquad filter, a current-mode multiplier/divider and floating inductance simulator are included. They occupy only single CCCDTA.

Keywords: Current controlled, CDTA, Biquad filter, Multiplier, Divider, Inductance simulator

1. INTRODUCTION

In the last decade, there has been much effort to reduce the supply voltage of electronic circuits. This is due to the command for portable and battery-powered equipment. Since a low-voltage operating circuit becomes necessary, the current-mode technique is ideally suited for this purpose more than the voltage-mode one. Consequently, there is a growing interest in synthesizing the current-mode circuits because of more their potential advantages such as larger dynamic range, higher signal bandwidth, greater linearity, simpler circuitry and low power consumption [1-2]. Many active elements able to function in current-mode such as OTA, current conveyor and Current Differencing Buffered Amplifier (CDBA), have been introduced to response these demands.

Recently, a reported 5-terminals active element, namely Current Differencing Transconductance Amplifier (CDTA) [3], seems to be a versatile component in the realisation of a class of analog signal processing circuits, especially analog frequency filters [4-5]. It is really current-mode element whose input and output signals are currents. It should also be noted here that, the CDTA offers wider frequency bandwidth advantages as compared to its close relative, the CDBA [6]. In addition, it can also adjust the output current gain. However, from our investigations, there are seen that the CDTA can not be controlled the parasitic resistances at two current input ports so when it is used in a circuit, it must unavoidably require some external passive components, especially the resistors. This makes it not appropriate for IC implementation due to occupying more chip area.

The purpose of this paper is to design and synthesize a modified-version CDTA, which is newly named Current Controlled Current Differencing Transconductance amplifier (CCCDTA). The parasitic resistances at two current input ports can be controlled by an input bias current, then it does not need a resistor in practical applications. The performances of proposed CCCDTA are illustrated by PSPICE simulations, they show good agreement as mentioned. Some example applications as a universal filter, multiplier/divider and floating inductance simulator are comprised.

Fig.1: The CCCDTA (a) Symbol (b) Equivalent circuit

1,2 The authors are with Department of Teacher Training in Electrical Engineering, Faculty of Technical Education, King Mongkuts Institute of Technology North Bangkok, Bangsue, Bangkok, 10800, THAILAND Email: mts@kmitnb.ac.th, jnaiz2004@yahoo.com

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2. CIRCUIT CONFIGURATION

2.1 Basic Concept of CCCDTA

CCCDTA properties are similar to the conventional CDTA, except that input voltages of CCCDTA are not zero and the CCCDTA has finite input resistances \( R_p \) and \( R_n \) at the \( p \) and \( n \) input terminals, respectively. These parasitic resistances are equal and can be controlled by the bias current \( I_{B1} \) as shown in the following equation

\[
\begin{bmatrix}
V_p \\
V_n \\
I_z \\
I_x
\end{bmatrix} = \begin{bmatrix}
R_p & 0 & 0 & 0 \\
0 & R_n & 0 & 1 \\
1 & -1 & 0 & 0 \\
0 & 0 & 0 & \pm g_m
\end{bmatrix} \begin{bmatrix}
I_p \\
I_n \\
V_x \\
V_z
\end{bmatrix}
\]  

(1)

When

\[ R_p = R_n = \frac{V_T}{2I_{B1}} \]  

(2)

and

\[ g_m = \frac{I_{B2}}{2V_T}. \]  

(3)

Where \( g_m \) is the transconductance of the CCCDTA and \( V_T \) is the thermal voltage. The symbol and the equivalent circuit of the CCCDTA are illustrated in Fig. 1(a) and (b), respectively.

\[ \text{Fig. 2: Class AB translinear loop} \]

2.2 A current differencing circuit which has finite input resistances

Fig. 2 displays a class AB translinear loop, which is used as input section. When all transistors are considered to be matched elements and working in saturation mode. The following currents can be obtained

\[ I_2 = I_{B1}e^{(V_n/V_T)} \]  

(4)

\[ I_5 = I_{B1}e^{- (V_n/V_T)} \]  

(5)

Due to

\[ I_n = I_2 - I_5 \]  

(6)

Substituting Eqns. (4) and (5) into (6), it yields

\[ I_n = 2I_{B1} \sinh(V_n/V_T) \]  

(7)

Since \( \sinh(V_n/V_T) \equiv V_n/V_T \), we will obtain

\[ R_n = R_p = \frac{V_T}{2I_{B1}}. \]  

(8)

The current differencing circuit which has finite input resistances is shown in Fig. 3. The circuit implementation consists of mixed translinear loop \((Q_1 - Q_6)\). The mixed loops are DC biased by \( I_{B1} \) using current mirrors \((Q_7 - Q_{10}) \) and \((Q_{14} - Q_{16})\). The p and n terminal resistances can be obtained by Eqn. (8). The output z-terminal that generates the current difference of p and n terminal is realized using transistors \( Q_{11} - Q_{13} \) and \( Q_{17} - Q_{21} \).

\[ \text{Fig. 3: A current differencing circuit which has finite input resistances} \]

The output resistance looking into the z terminals can be respectively expressed as

\[ r_z \approx \frac{r_{ce}}{2} / \beta r_\pi. \]  

(9)

2.3 Transconductance Amplifier

In this section, a simple differential pair amplifier \([7]\) is employed to achieve simpler circuit description of the proposed CCCDTA as shown in Fig. 4.

From Fig. 4, transistors \( Q_{22} \) and \( Q_{23} \) function as a differential amplifier to convert an input voltage to an output current. \( Q_{24} \) and \( Q_{25} \) work as a simple current mirror when \( I_{B2} \) is an input bias current. When \( V_{in} \) is applied, this makes \( I_{C22} \) and \( I_{C23} \) flowing in \( Q_{22} \) and \( Q_{23} \), respectively. The relationship of \( I_o \) and \( V_{in} \) of the transconductance amplifier is given by \([12]\)

\[ I_o = I_{B2} \tanh \left( \frac{V_{in}}{2V_T} \right). \]  

(10)

Where \( (V_{in}/2V_T) \equiv V_{in}/2V_T \), for small-signal, it yields

\[ I_o = I_{B2} \frac{V_{in}}{2V_T} \]  

(11)

or

\[ I_o = g_m V_{in} \]  

(12)
Where \( g_m = \frac{I_{B2}}{2V_T} \).

The output resistance looking into the x terminals can be respectively expressed as

\[ r_x \approx \frac{r_{ce}}{2}. \] (13)

When \( r_{ce} \) is the collector-emitter resistance seen at the mentioned output terminal.

3. PERFORMANCE ANALYSIS

3.1 Area mismatch

From Section 2.2, emitter area mismatch errors from transistors will mostly affect the operation of the translinear circuit. For this reason, symmetrical and common centroid layout techniques should be employed for the transistors within the translinear loop. Good layout techniques will also help reduce error due to process and thermal variations.

3.2 Finite output resistance

If the effects of base-width modulation are taken into account, the collector current of the transistor is changed to

\[ I_c = I_{s4} e^{\frac{(V_{BE}/V_T)}{1 + V_{CE}/V_A}} \] (14)

Where \( V_A \) is the Early voltage of the transistor. Thus

\[ V_{BE} = V_T \ln \left| \frac{I_c}{I_{s4}k_4} \right|. \] (15)

Where \( k_i = 1 + \frac{V_{CE}}{V_A} \). The Early voltage effect appears like an area mismatch.

The intrinsic input resistances with considering the finite output resistances of the transistors are modified to

\[ R_n = R_p = \frac{V_T}{2I_{B1}} + \frac{V_T}{I_n} \ln \left( \frac{I_{s4}k_4}{I_{s5}k_5} \right). \] (16)

Where \( k_i = 1 + \frac{V_{CE}}{V_A} \). From Eqn. (16), it should be observed that the second term is the error originated from the Early voltage transistor mismatch compared to Eqn. (8). Consequently, keeping values of \( I_{s4}k_4 \) and \( I_{s5}k_5 \) to be equal must be strictly considered.

3.3 Finite beta

Errors due to finite \( \beta \) occur frequently in translinear circuits, since a bipolar transistor needs to be provided with base current. This base current is often taken directly from an input or output current source, and results in error terms in the circuit transfer function. These \( \beta \) errors are due to the circuit implementation, rather than being an inherent error in the translinear circuit principle. Any series base resistance (\( R_{bb} \)) also affects the operation of a transistor circuit, since it ruins the exponential current-voltage relation in such

\[ V_{BE} = V_T \ln \left( \frac{I_c}{I_s} \right) + \frac{I_c R_{bb}}{\beta}. \] (17)

In similar, the intrinsic input resistances with considering the finite beta of the transistors are changed to

\[ R_n = R_p = \frac{V_T}{2I_{B1}} + \frac{R_{bb}}{\beta_4} \left( \frac{R_{bb}}{\beta_4} - \frac{R_{bb}}{\beta_5} \right). \] (18)
Where $\beta_i$ is the DC current gain of $i^{th}$ transistor. From Eqn. (18), it should be concluded that the second term is the error from finite beta transistor mismatch compared to Eqn. (8). Thus, keeping ratio of $R_{bb}/\beta_4$ and $R_{bb}/\beta_5$ to be equaled is preferred.

To simplify the analysis of translinear circuits, it is usual to neglect transistor base currents. However, a full circuit analysis including base current errors is often useful for comparing alternative circuit topologies.

3.4 Effects from non-ideal characteristics of CCCDTA

There are some non-ideal characteristics in the parameters of CCCDTA. One of them is the gain of amplifiers. The CCCDTA comprises a current differencing amplifier and a transconductance amplifier. Due to parasitic elements and non-ideal characteristics of active devices, the output currents of practical CCCDTA are written as

$$i_Z = \alpha_p i_p - \alpha_n i_n.$$

and

$$i_X = \beta g_m v_Z.$$

Where $\alpha$ and $\beta$ are the gains of the current differencing circuit and transconductance amplifier, respectively. In practical design, these errors should be carefully considered to achieve these factors to be close to unity as much as possible.

4. SIMULATION RESULTS

To prove the performances of the proposed CCCDTA, the PSPICE simulation program was used for the examination. The PNP and NPN transistors employed in the proposed circuit in Fig. 5 were simulated by respectively using the parameters of the PR200N and NR200N bipolar transistors of ALA400 transistor array from ATT [8] with $\pm 1.5$V supply voltages. Fig. 6 depicts the parasitic resistances at $p$ and $n$ input terminals when $I_{B1}$ is varied. We can found that the proposed CCCDTA prefers a wide range of input parasitic resistances over 3 decades.

Fig. 7 displays DC transfer characteristic of the proposed CCCDTA, when $I_{B1} = 50\mu A$. So it is clearly seen that it is linear in range of $-60\mu A \leq I_n(I_p) \leq 60\mu A$ and can be adjusted. The offset current is shown in Fig. 8, when $I_{B1}$ is varied from $0 - 100\mu A$. , we can found that the maximum output offset current is about $1\mu A$.

Fig. 9: Transconductance value relative to $I_{B2}$

A wide range of transconductance controllability can be achieved as shown in Fig. 9 when $I_{B2}$ is varied from $1nA - 10mA$. It should be observed that the linear controllability of the transconductance is more than 6 decades. Fig. 10 shows the transient responses of the CCCDTA, this result confirms that the switching time delay of the CCCDTA is approximately $15ns$. Moreover, the bandwidths of output terminals are shown in Fig. 10. The 3dB - of the current gain $I_z/I_n$, $I_z/I_p$, $I_x/I_n$ and $I_x/I_p$ are respectively located at $49MHz$, $65MHz$, $170kHz$ and $170kHz$, when $I_{B1} = I_{B2} = 100\mu A$.

From Fig. 11, it can be found that the frequency responses at the X terminal is narrower than those at the Z terminal, this is due to signal transmission
from the Z to X terminal of OTA. The summarized characteristics of the proposed CCCDTA can be seen in Table 1.

Table 1: Conclusions of CCCDTA parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply voltage</td>
<td>±1.5V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>1.23mW</td>
</tr>
<tr>
<td>-3dB Bandwidth</td>
<td>49MHz (Iz/In), 65MHz (Ix/Ip), 170kHz (Ix/Ip)</td>
</tr>
<tr>
<td>Input current linear range</td>
<td>-60 µA to 60 µA</td>
</tr>
<tr>
<td>Rn and Rp ranges</td>
<td>10Ω-47.2kΩ</td>
</tr>
<tr>
<td>Input bias current range for controlling Rn and Rp</td>
<td>1µA-1.4mA</td>
</tr>
<tr>
<td>Transconductance</td>
<td>50S-51mS</td>
</tr>
<tr>
<td>Input bias range for controlling transconductance</td>
<td>1n-8mA</td>
</tr>
<tr>
<td>Switching time delay</td>
<td>15ns</td>
</tr>
<tr>
<td>Rz</td>
<td>73.53kΩ</td>
</tr>
<tr>
<td>Rx</td>
<td>76.67kΩ</td>
</tr>
</tbody>
</table>

Fig. 12: Universal biquad filter based on the CCCDTA

5. APPLICATION EXAMPLES

To confirm the validity of the proposed building block, some applications are given here to demonstrate and prove the performances of the applications of the proposed element.

5.1 Current-mode biquad filter

The first application of the proposed CCCDTA is a current-mode biquad filter shown in Fig. 12. It employs only one active element and 2 grounded capacitors, which is easy to fabricate, differing from previous circuits [9-10]. Straightforwardly analyzing the circuit in Fig. 12 and using CCCDTA properties in section 2, the transfer functions of the network can be obtained as

\[
\frac{I_{HP}}{I_{in}} = \frac{s^2 + s \frac{1}{C_1 R_n} + \frac{g_m}{C_1 C_2 R_n}}{s^2 + \frac{1}{C_1 R_n} + \frac{g_m}{C_1 C_2 R_n}}, \quad (21)
\]

\[
\frac{I_{LP}}{I_{in}} = \frac{g_m/C_1 C_2 R_n}{s^2 + \frac{1}{C_1 R_n} + \frac{g_m}{C_1 C_2 R_n}}, \quad (22)
\]

\[
\frac{I_{BR}}{I_{in}} = \frac{g_m/C_1 C_2 R_n}{s^2 + \frac{1}{C_1 R_n} + \frac{g_m}{C_1 C_2 R_n}}, \quad (23)
\]

\[
\frac{I_{AP}}{I_{in}} = \frac{s^2 - s/C_1 R_n + g_m/C_1 C_2 R_n}{s^2 + \frac{1}{C_1 R_n} + \frac{g_m}{C_1 C_2 R_n}}, \quad (24)
\]

The confirmed result can be seen in Fig. 13. From Eqns. (21) and (25), setting \( C_1 = C_2 = C = 10\mu F \), \( I_{B1} = I_{B2} = 50\mu A \) and using the CCCDTA properties, then the pole frequency \( \omega_o \) and the quality factor \( Q \) are

\[
\omega_o = \sqrt{\frac{I_{B1} - I_{B2}}{V_T C}}, Q = \frac{1}{2} \sqrt{\frac{I_{B2}}{I_{B1}}} \quad (26)
\]
It should be observed from Eqn. (26) that the pole frequency and the quality factor can be orthogonally adjusted. It means that the pole frequency can be tuned by both $I_{B1}$ and $I_{B2}$ with keeping $I_{B2}/I_{B1}$ ratio constant, as shown in Fig. 14.

If non-idea characteristics of the CCCDTA as explained in Section 3 are considered, the pole frequency and the quality factor of the proposed filter are changed to

$$\omega_0 = \frac{1}{V_T C} \sqrt{\beta z \alpha_n I_{B1} I_{B2}}, \quad Q = \frac{1}{2} \sqrt{\beta z \alpha_n I_{B2} / I_{B1}}$$

(27)

If these gains are close to unity, Eqn. (27) can be considered to be equal to Eqn. (26).

5.2 Current-mode Multiplier/Divider

The multiplier/divider based on the CCCDTA is shown in Fig. 15. It employs only single CCCDTA, which contrasts to ordinarily proposed circuits [10-11]. From routine analysis using the CCCDTA properties, we will get output current $I_O$ as

$$I_O = \frac{I_A I_C}{8I_B}. \quad (28)$$

In similar, if non-idea characteristics of the CCCDTA are considered, the output current of the multiplier/divider is modified to

$$I_O = \frac{\beta z \alpha_n I_A I_C}{4(1 + \alpha_p)} I_B. \quad (29)$$

If these gains are designed to be close to unity, Eqn. (29) can be considered to be equal to Eqn. (28). It is clearly seen that $I_o$ is a result of either, multiplying of $I_A$ and $I_C$, or dividing of $I_A$ and $I_B$. Due to being a positive value of $I_B$ and $I_C$, the proposed circuit can be a 2 quadrant multiplier/divider. Fig. 16(a) and (b) show the DC response characteristics of multiplication, where $I_B = 5 \mu A$ and division of the proposed circuit, where $I_C = 20 \mu A$, respectively.

Fig. 17(a) shows the transient responses of multiplication, where $I_A$ and $I_C$ were set to be a sinusoidal signal $20 \mu A_{p-p}$ at 10kHz frequency and triangular signal $20 \mu A_{p}$ with 1kHz frequency, respectively. Fig. 16(b) shows division of the proposed circuit, where $I_A$ and $I_C$ were set to be $40 \mu A$ and $B I$ was a triangular signal with frequency of 1kHz. Furthermore, the claimed temperature-insensitivities of the proposed circuit are confirmed as shown in the results of DC responses in Fig. 18 and in that of transient responses in Fig. 19.
Fig. 17: Transient responses of the multiplier/divider

Fig. 18: Output current deviations due to temperature variations of the multiplier/divider for DC responses

Fig. 19: Output current deviations due to temperature variations of the multiplier/divider for transient responses

Fig. 20: Floating inductance simulator using CCCDTA

5.3 Floating inductance simulator

Fig. 20 depicts the proposed floating inductance simulator, where $I_{B1}$ and $I_{B2}$ are input bias currents of CCCDTA. Circuit description of voltage buffers are shown in Fig. 21.

Considering the circuit in Fig. 20 and using CCCDTA properties in section 2.1, we will receive

$$I_z = V_1 - V_2 \frac{R}{sC}.$$  

Where $R_n = R_p = R$, the voltage at $z$ terminal can be shown as

$$V_z = \frac{I_z}{sC} = \frac{V_1 - V_2}{sCR}. \quad (31)$$

The output current of CCCDTA can be found as

$$I_x = I_L = \frac{gm(V_1 - V_2)}{sCR}. \quad (32)$$
From Eqn. (32), an input impedance of the circuit can be written as

\[ Z_{in} = \frac{V_1 - V_2}{I_L} = \frac{sCR}{g_m}. \]  

(33)

From Eqn. (33), it is obvious that the circuit shown in Fig. 20 simulates a floating inductance with a value

\[ L_{eq} = \frac{CR}{g_m}. \]  

(34)

It is clearly seen that, from Eqn. (34), the inductance value \( L_{eq} \) can be adjusted electronically by either \( I_{B1} \) or \( I_{B2} \).

For non-ideal case, the \( I_z \) and \( I_x \) of CCCDTA can be respectively characterized by

\[ I_z = \alpha p I_p - \alpha n I_n \]  

(35)

and

\[ I_x = \beta_2 g_m V_z. \]  

(36)

While the \( V_o \) of voltage buffer can be characterized by

\[ V_o = \beta_b V_{in}. \]  

(37)

Where \( \alpha \) and \( \beta \) are current gain error and voltage gain error of CCCDTA and voltage buffer, respectively. Taking into account, \( \alpha \) and \( \beta \) effect on the circuit in Fig. 20, it can be found that

\[ I_L = \frac{g_m \beta_2}{sCR} (\alpha_n \beta_1 V_1 - \alpha_p \beta_2 V_2). \]  

(38)

Where \( \alpha \beta_1 = \alpha p \beta_2 = \varepsilon \), the input impedance can be written as

\[ Z_{in} = \frac{V_1 - V_2}{I_C} = \frac{sCR}{\varepsilon g_m \beta_z}. \]  

(39)

From Eqn. (39), for non-ideal consideration, the circuit in Fig. 20 simulates a floating inductance with a value

\[ L_{eq} = \frac{sCR}{\varepsilon g_m \beta_z}. \]  

(40)

If these error factors are close to unity, the deviations of the inductance values in Eqn. (40) can be neglected.

Fig. 21: Voltage buffer used in Fig. 20

Fig. 22: Typical waveforms of voltage and current of the proposed inductor simulator

Fig. 23: Series RLC resonant circuit

To illustrate an application of the floating inductor simulator, it is employed in an RLC series-resonant circuit shown in Fig. 23, where \( V_{in} = 10mV \). The frequency responses of output current \( I_o \) for different \( I_{B2} \) are shown in Fig. 24.

Fig. 24: Simulated current characteristics of the resonant circuit in Fig. 7 when \( I_{B2} \) is varied

Fig. 25: The impedance values relative to frequency of the simulator
The impedance of the simulator relative to frequency, which is compared to ideal inductor, is also shown in Fig. 25. In addition, Fig. 26 shows impedance values relative to frequency of the simulator with different $I_{B2}$. It is confirmed that the proposed inductor enjoys several features; for instance, electronic tunability, use of grounded capacitor which can be easily fabricated for VLSI, free from component matching. Moreover, the proposed circuit has simpler circuit description than the recently previous works [13-20].

6. CONCLUSIONS

A building block for analog signal processing circuit design, called as CCCDTA, has been introduced in this paper. The usability has been proven by the simulation and application examples. They consume few numbers of components while electronic controllability is still available, which differs from the recently proposed circuits. This novel element is very appropriate to realize in commercially-purposed integrated circuit. Our future work is to find more applications of the CCCDTA, such as oscillator, rectifier, amplifier, filter, etc., emphasizing on current-mode signal processing circuits.

References


Montree Siripruchyanun received the B. Tech. Ed. degree in electrical engineering from King Mongkuts Institute of Technology North Bangkok (KMITNB), the M.Eng. and D. Eng. degree both in electrical engineering from King Mongkuts Institute of Technology Ladkrabang (KMITL), Bangkok, Thailand, in 1994, 2000 and 2004, respectively. He has been with Faculty of Technical Education, KMITNB since 1994. Presently, he also functions as Deputy Director of Science and Technology Research Center (STRC) and is with Department of Teacher Training in Electrical Engineering as an Assistant Professor, KMITNB. His research interests include analog-digital communications, analog signal processing and analog integrated circuit. He is a member of IEEE (USA), IEICE (Japan), and ECTI (Thailand).

Winal Jaikla received the B. Tech. Ed. degree in telecommunication engineering from King Mongkuts Institute of Technology Ladkrabang, Thailand in 2002 and Master of Tech. Ed. in electrical technology from King Mongkuts Institute of Technology North Bangkok (KMITNB) in 2004. Now, he is working toward Ph. D. in Electrical Education at KMITNB. He has been with Electric and Electronic Program, Faculty of Industrial Technology, Suan Sunandha Rajabhat University, Bangkok, Thailand since 2004. His research interests include electronic communications, analog signal processing and analog integrated circuit. He is a member of ECTI (Thailand).