

# Switching Activity Based Method for Minimizing Testing Power in Digital Circuits

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## ABSTRACT

Optimization of testing power is a major significant task to be carried out in digital circuit design. Low power VLSI circuits dissipate more power during testing when compared with that of normal operation. In this paper a novel method is proposed to reduce the testing power and total energy by reordering the sequence of test vectors for minimum switching activity of the Circuit Under Test (CUT). Graph theory concept is used to develop the reordering algorithm which is based on heuristic approach to find near optimal solution for the problem. Fault coverage of the CUT is not affected in this algorithm. The reduction of power dissipation and total energy during testing leads to increase in reliability of the circuit. Experimental results of the proposed algorithm with ISCAS85 benchmark circuits show that the switching activity is reduced significantly compared to existing works.

**Keywords:** ATPG, Switching Activity, Reordering, Heuristics, Test Power

## 1. INTRODUCTION

Power dissipation has become a critical design concern in recent years driven by the emergence of portable devices in mobile applications. This is applicable not only to design power but also for testing power. In testing process, if test vector sets are not optimized for power, even low power circuits dissipate two fold power under test as they do at normal operating condition [1]. When the circuit is tested with pseudo-random patterns, consecutive input test vectors are statistically independent and this results in increased switching activity in the circuit during testing. Since in CMOS circuits energy is primarily consumed due to switching activity, the average power consumption during testing is significantly higher than normal mode of operation.

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The correlation between consecutive test vectors applied to a circuit is to be considered for testing of VLSI circuits. The correlation[2] for test vectors generated by an Automatic Test Pattern Generator (ATPG) is very low, since a test vector is generated for a given target fault without any consideration of the previous vector in the test sequence. Excessive switching activity due to low correlation between consecutive test vectors can cause several problems.

First, since heat dissipation in a CMOS circuit is proportional to switching activity, the circuit can be permanently damaged when the circuit experiences more switching activity[2,3] during its operation.

Second, it has been observed that metal migration or electro-migration causes the erosion of conductors and subsequent failure of circuits [2,4]. Since temperature and current density are major factors that determine electro-migration rate, elevated temperature and current density caused by excessive switching activity during test application can severely influence the reliability of CUT.

Finally, to test a bare dice, power must be supplied during the period of test through probes which typically have higher inductance than power and ground pins of a circuit package[2]. Hence, the bare dice under test will experience higher power/ground noise which is given by  $Ldi/dt$ , where L is the inductance of power and ground lines.

In this paper, a novel method is proposed to reduce the testing power by reordering the sequence of test vectors for minimum switching activity of the CUT. A set of test vectors are applied to the CUT during testing. The order of application of vectors changes the total switching activity of the circuit. Lowest switching activity for a given order of test vectors is called minimum switching activity of the CUT. The order is called reordered test set. The test power obtained by applying the reordered test set is regarded as optimum test power.

The key parameter in testing “coverage” is not altered and significant improvement in minimizing switching activity during testing is achieved in the proposed method. The reordering algorithm is applied as off-line with respect to the testing process. Hence the testing time, effectiveness of testing, functionality of the system is not affected by the algorithm.

The paper is organized as follows. Section 2 discusses about background and related work for the proposed work. Problem definition and algorithm are

discussed in section 3. Section 4 describes the implementation and results of proposed algorithm. The paper is concluded in the section 5. Finally the section 6 is added with references.

## 2. BACKGROUND OF THE WORK

### 2.1 Energy and Power Modelling

The Power dissipation in CMOS technology [2, 5, 6] can be classified into static and dynamic. Static dissipation is due to leakage current that has small magnitude about 20% in digital system. Hence, for such circuits, the dynamic dissipation [7, 5] is the dominant term with 80% of total power. Dynamic dissipation is due to short circuit current and charging and discharging of load capacitances during output switching from one logic level to another level in the signal lines or nodes of the circuit.

As discussed in [8], three parameters are important for evaluating the power properties of a CUT during testing.

- The consumed *energy* directly corresponds to the switching activity generated in the circuit during test application, and has impact on the battery lifetime during remote testing.
- The *average power* consumption is given by the ratio between the energy and the test time. This parameter is even more important than the energy as hot spots and reliability problems may be caused by constantly high power consumption.
- The *peak power* consumption corresponds to the highest switching activity generated in the CUT during one clock cycle. The peak power determines the thermal and electrical limits of components and the system packaging requirements. If the peak power exceeds certain limits, the correct functioning of the circuit is no longer guaranteed.

The average energy consumed at node  $i$  per switching is given in (1)

$$E_{ave} = 1/2C_L V^2 \quad (1)$$

where  $C_L$  is the equivalent load capacitance and  $V$  the power supply voltage in CMOS logic. Therefore, a good approximation of the energy consumed in a period  $T$  is given in (2)

$$E_T = 1/2C_L S_i V^2 \quad (2)$$

where  $S_i$  is the number of switching during the period. In the process of testing, the energy consumed in the circuit after application of a pair of successive input test vectors  $(t_{k-1}, t_k)$  can then be expressed by equation (3)

$$Et_k = 1/2C_L V^2 \sum_i S(i, k) \quad (3)$$

where  $i$  ranges all the nodes of the circuit and  $S(i, k)$  is the number of switching provoked by  $t_k$  at node

$i$ . Consider now a pseudo-random test sequence of length  $n$ , where  $n$  is the test length required to achieve the targeted fault coverage, the total energy consumed in the circuit during application of the complete test sequence is given in (4).

$$E_{total} = 1/2C_L V^2 \sum tk \sum_i S(i, k) \quad (4)$$

Let us denote the clock period as  $T$ . By definition, the instantaneous power is the power consumed during one clock period.

The peak power consumption corresponds to the maximum of the instantaneous power consumed during the test session. Therefore, it corresponds to the highest energy consumed during one clock period, divided by  $T$ . More formally, it is given in (5).

$$P_{peak} = Max(Et_k/T) \quad (5)$$

where  $k$  varies 1 to  $n$ .

Finally, the average power consumed during the test session is the total energy divided by the test time, and is given in (6).

$$P_{ave} = E_{total}/(nT) \quad (6)$$

It is understood from the above expressions of the power and energy consumption, for a given CMOS technology with specified supply voltage of the circuit design, switching  $S_i$  of node  $i$  is the only parameter that affects the power and energy consumption. Hence the proposed work aims at reducing the switching activity in the CUT to minimize the heat dissipation during testing.

### 2.2 Related Work

Many techniques are discussed in literatures[2, 4, 5, 9-17] for reducing testing power. The earlier work[9] of this paper used Hamming Distance between two successive test vectors to reduce switching activity. The test vectors are reordered for minimum total hamming distance of the complete test set. This Hamming Distance approach is based on the concept that the internal switching activity is more or less depending on the hamming distance at the input of the circuit. This may not be true for all the circuits and the switching activity is depending on the logic gates that are used to construct the circuit. The methods proposed in [10] and [11] are used to reduce testing power using switching activity concept. Both the methods are based on Genetic Algorithm approach in which the fault coverage is altered while reordering is carried out. This will degrade the performance of fault simulation algorithm or ATPG. In [2] new ATPG was devised based on PODEM algorithm by considering switching activity of the CUT. Test scheduling method was proposed in [12] which aims at minimizing energy consumption and test application time by considering the switching activity in

the overlapping regions of the sub-circuits under test. Three methods were discussed in [5] for test power optimization for delay faults and stuck-at-faults. Hamming distance approach and its drawbacks also discussed in the paper [5]. The technique used in [13] is also based on hamming distance concept but switching activity reduction is very less when compared with the proposed work. Techniques for minimizing power dissipation during testing of combinational and scan circuits are discussed in [4] where the Minimum Spanning Tree (MST) algorithms is used to minimize the switching activity of the CUT. An algorithm is devised in [14] which minimizes the power dissipation in scan cells during the capture mode of the scan based testing. Don't care(X) filling algorithm is used to reduce the transitions between the given test vector and its response. Though this method is effective, it reduces only the capture mode power which is a small part of total testing power in modern VLSI circuits. A novel flip-flop design is proposed in [15] to reduce the instantaneous power by distributing the logical activity throughout the scan clock cycle in scan based testing. In [16], a new scan architecture called "Jump Scan" is proposed to reduce the test power in scan cells. The penalties of this method are area overhead and speed degradation. In practice, area overhead can be traded off with testing power but speed degradation or test time can not be traded off with testing power. The paper [17] discussed two methods used for reordering of test vectors in order to reduce the dynamic power dissipation during testing of combinational circuits. The Two search methods 2-opt heuristic and a genetic algorithm based approach have been applied and results obtained for combinational circuits. These types of reordering algorithms perform well when heuristic approach is used.

Generally, the nature of any VLSI system is sequential logic whose testing power is due to power dissipation in Combinational Circuit, Scan cells, and Clock Tree. Since Combinational circuit occupies more area, it consumes more power during testing. Hence the proposed reordering algorithm is meant for minimizing testing power and energy in Combinational part of VLSI system. The problem and its solution for the proposed work are described in the next section.

### 3. PROBLEM FORMULATION

The power dissipation during testing [1] is minimized by reducing the number of transitions in the circuit. Usually test vectors are in random and hence it is necessary to rearrange the order of occurrence of test vectors so that minimum switching activity between successive test vectors is obtained.

As mentioned in section 2, the problem of minimizing switching power is solved by graph theory using Hamiltonian path [18] technique. Graph  $G(V, E)$  is defined with  $V$  nodes and  $E$  edges. The problem

is formulated by considering the test vector as node and switching activity between them as edge cost of the graph. The graph considered here is complete graph [18] whose all the nodes are connected each other with edges. Adjacency matrix for the graph is represented by switching activity matrix  $swa[i][j]$  of order  $n \times n$ . The matrix element  $swa[i][j]$  represents switching activity in the CUT when  $j^{th}$  test vector is applied after  $i^{th}$  test vector.

In this graph, the Hamiltonian path is a path connected by all nodes with minimum total edge cost. Reordering algorithm is used to construct the Hamiltonian path, which is resultant reordered test vector set with minimum total switching activity in CUT. Hence this path offers less number of transitions in the circuit which in turn results in reduced power dissipation in the CUT during testing [19]. Heuristic approach is used in the algorithm to find more sub-optimal sequences. The more suboptimal solutions can be obtained when two or more values of switching activity matrix  $swa[i][j]$  are identical. These solutions are called heuristic based sub-optimal solutions.

The reordering algorithm used to minimize the switching activity during testing is given as follows.

#### Reordering Algorithm:

The various parameters used in the algorithms are as follows:

$t_1, t_2, \dots, t_n$  be  $n$  test vectors with  $m$  bits each.

$T = \{1, 2, \dots, k \dots n\}$  where  $k$  represents  $k^{th}$  position in the vector set generated by ATPG.

$R$  is a set to store ordered test vector sequence.

$Q$  is a set to store  $T - R$ .

$swa\_init[x]$  is one dimensional array of order  $1 \times n$  and represents initial switching activity of CUT for every test vector when applied separately.

**Step 1:** Select a test vector  $x$  such that  $swa\_init[x]$  is minimum in the array  $swa\_init[x]$ . Add  $x$  to set  $R$ .

**Step 2:** Select a test vector  $y_{min}$  such that  $swa[x][y_{min}]$  is minimum in the array.

**Step 3:** Add  $y_{min}$  to  $R$ ;  $Q \leftarrow T - R$ ;  $x_{min}y_{min}$ .

**Step 4:** From the array  $swa[x_{min}][j]$  when  $j$  varies as in  $Q$ , find  $y_{min}$  so that  $swa[x_{min}][y_{min}]$  is the smallest value. Go to step 3.

**Step 5:** In the step 4, if  $swa[x_{min}][j]$  has more than one smallest value then such number of reordered sequence will be generated for every  $x_{min}$ . These sequences are called as sub-optimal sequences.

Finally the set  $R$  will have reordered test vector sequence with minimum switching activity in the CUT. When the reordered test vectors are applied, the Total Switching Activity (TSA) of the circuit is calculated by the given equation (7),

$$SWA_{total} = swa\_init[R[1]] + \sum_{i=1}^{n-1} swa[R][i][R[i+1]] \quad (7)$$

where  $R[i]$  is  $i^{th}$  positional test vector number stored in the set  $R$ .

The procedure for testing process using reordering algorithm is described here for any VLSI circuit.

1. Consider a digital circuit with  $p$  inputs and  $q$  outputs.

2. Generate all the test vectors to detect the entire single stuck at faults [1] of the circuit. The test vectors may be having don't care. Let  $n$  be the number of test vectors generated by ATPG.

3. Find the internal switching activity between each and every test vector by applying them in proper sequence to the CUT and load the same in array  $swa$  of size  $n \times n$ . Let  $swa[i][j]$  be the array element that gives switching activity between  $i^{th}$  and  $j^{th}$  test vector.

4. Find the internal switching activity of every test vector by applying them in the CUT separately and load the same in array  $swa\_init$  of size  $n \times 1$ . Let  $swa\_init[i]$  be the array element that gives initial switching activity when  $i^{th}$  test vector alone is applied.

5. Apply reordering algorithm to find the re-ordered test vector sequence with minimum total switching activity.

6. Then the reordered test sequence is used either to design the Test Pattern Generator(TPG) for generating the same sequence in BIST architecture or to program the Automatic Test Equipment(ATE) for external testing.

To understand the above procedure, illustration is made with simple ISCAS85[20] benchmark circuit  $c17$  to show the effectiveness of the proposed algorithm. The test vector set that used to detect the entire single stuck at faults is given in Table 1. This is generated by ATPG tool called ATALANTA[21]. The test set consists of 6 vectors and are serially numbered from  $t_1$  to  $t_6$  as given in the table. Total Switching Activity of the circuit is 52 when the test set is applied in the same sequence. The switching activity arrays  $swa\_init[]$  and  $swa[i][j]$  are constructed by applying the test set to the CUT. These are given as in Table 2 and Table3 respectively. On application of reordering algorithm to these matrices, two sub-optimal solutions are developed when starting with test vector  $t_3$  whose  $swa\_init[3]=2$  which is minimum. This is due to the two similar values in the 5th row of  $swa[i][j]$  matrix. Hence two paths are developed from test vector  $t_5$  to get two sub-optimal solutions. The solutions and their TSA are given as follows:

Solution1.  $t_3 - t_6 - t_5 - t_2 - t_4 - t_1$

TSA = 29

Solution2.  $t_3 - t_6 - t_5 - t_4 - t_2 - t_1$

TSA = 27

Though it starts with only one test vector  $t_3$ , two solutions are obtained when heuristic approach is incorporated in the algorithm. Here the TSA of sub-optimal solution2 is lesser than that of solution1. Hence solution2 is optimized reordered test set with minimum switching activity. This shows that 48% of TSA is reduced in the ordered test set over the unordered test set.

**Table 1:** Test vectors for  $c17$  circuit

Test vector set (n=6)	No.
11100	$t_1$
11111	$t_2$
00000	$t_3$
01110	$t_4$
01011	$t_5$
10001	$t_6$

**Table 2:** Initial switching activity array  $swa\_init[]$  for  $c17$

$t_1$	$t_2$	$t_3$	$t_4$	$t_5$	$t_6$
15	22	2	18	12	12

**Table 3:** Switching activity array  $swa[][]$

	$t_1$	$t_2$	$t_3$	$t_4$	$t_5$	$t_6$
$t_1$	0	7	7	7	6	7
$t_2$	5	0	8	4	9	8
$t_3$	7	14	0	10	7	4
$t_4$	7	4	4	0	7	8
$t_5$	9	7	7	7	0	5
$t_6$	7	10	4	12	5	0

#### 4. RESULTS AND DISCUSSIONS

The proposed low power testing algorithm is implemented using C Language and tested with benchmark circuits ISCAS85[18]. Each circuit is implemented using VHDL to perform the following tasks:

- (i) To realize the logic with zero delay model
- (ii) For single stuck-at fault simulation
- (iii) To calculate the total switching activity of the circuit during testing

The logic of benchmark circuit is realized in VHDL using structural or dataflow modeling with zero propagation delay. The fault simulation is carried out by simulating the VHDL code using the tool "Modelsim" with the test vectors generated in the ATPG. The special feature of the VHDL is ability to detect the 0 to 1 or 1 to 0 transitions occurred in the any signal line of the circuit. This is accomplished by VHDL attribute "signal'event" which is boolean type whose output is TRUE if signal got event (0 to 1 or 1 to 0) and FALSE otherwise. A counter is defined in the

VHDL code for every signal of the circuit and incremented by 1 for every event. Finally all the counters are added to find the total switching activity (transitions) in the circuit during the entire period of fault simulation. Fault simulation for unordered and ordered test set is carried out to find the total switching activity for the each case. Results show that switching activity of ordered test set is always less than that of unordered test set.

The reordering is carried out without modifying the binary pattern of test vectors and hence the fault coverage of CUT remains unchanged. The circuits are implemented with zero delay modelling and hence the glitches are not included in the work.

The results obtained for the benchmark circuits are tabulated in Table 4. Details of benchmark circuits such as Size(number of gates), number of test vectors(n) and fault coverage are given in the table. Total switching activity (TSA) and switching activity per test vector (SPT) for unordered and ordered test set are given for each circuit. As mentioned in section 2.1, TSA represents total energy and SPT represents the average power of the CUT, Table shows that an average of 39.34% improvement is achieved in reducing the TSA and SPT when reordering algorithm is applied. The time required to generate swa[ ][ ] matrix is also given in the last column. The time complexity for the generation is  $n^2-n$ . This is proportional to the number of test vectors (n) and size of the circuit. Since the generation of swa[ ][ ] and reordering are carried out as off-line only once during design of VLSI circuits, the time duration does not affect the testing time.

Table 5 depicts comparison results of previous phase of the proposed work[9]. Hamming distance concept was used in the previous phase of this work. The same reordering of test vectors was carried out to minimize the Hamming distance of whole test set. The total Switching activity is obtained and tabulated for both the concepts. This shows an average improvement of 13% is achieved when compared with previous phase.

As discussed in the section 1, Hamming distance approach does not give good results for all the circuits. So here four circuits (c17, c432, c1355, c6288) have improvement out of 6 circuits. There is no improvement for two circuits (c499 and c1908). This is because the logic of the circuits is dependent on the input change. Hence hamming distance approach gives better result for these two circuits than switching activity approach. More dependent implies that more transitions occurred for small change in the input(hamming distance). Most of the circuits are under the category of dependent on hamming distance and few circuits are under “more dependent” and “less dependent”. Hence only minimum average improvement is achieved in the switching activity approach.

Table 6 gives comparison results with existing methods [2, 4, 13] for TSA which represents total energy of the CUT. In [2] and [4], the results are given as average switching activity (number of switching activity per test vector). To find the TSA, average value is multiplied by the number of test vectors (n). The results show that up to 83% of improvement is achieved in switching activity reduction when compared to that of existing methods. In [2], a maximum improvement of 79.4% is obtained for the circuit C1908 and minimum of 10% is achieved for the circuit C2670. The average improvement of proposed method is 35% over that of [2]. In [4], two methods are proposed and out of which greedy method is better than christofides one. Here an average improvement of 41% is achieved over christofides method and 33% over greedy method. In the circuit C880, greedy method is better than the proposed approach with 6.4% of improvement. The same is applicable for another existing method[13] also with 26.8% improvement over the proposed method.

The results are obtained for average switching activity and tabulated in Table 7. This is calculated as number of switching activity per test vector. This corresponds to the average power of the CUT. The proposed algorithm reduces total, average and peak switching activity and hence their energy and power also. Table shows that methods proposed in [2] and [4] reduced the average switching activity for circuits c880, c2670, c5315 and c7552 when compared with proposed algorithm. But the reduction was achieved with the expense of up to 366% more number of test vectors than the proposed algorithm. In [2], the ATPG algorithm is modified to reduce the switching by adding more number of vectors. ATPG used in [4] was proposed by Larabee [22] that generates more test vectors than that of ATALANTA and MINTEST[23], which are used in this proposed work. In this reordering algorithm, more number of sub-optimal solutions are possible when n is higher value. For the other circuits in [2], the proposed algorithm gives better reduction of testing power. In [4], two methods are compared for average switching activity that shows an improvement of 23% and 16.2% is achieved respectively. Test vector overhead in [4] is upto 181% when compared with proposed method. This additional test vectors increase the both testing time and total energy of the CUT.

Table 8 gives the comparison results with existing methods in [17]. The results obtained in [17] are average value of 30 times simulation results. The results are compared for 8 benchmark circuits (ISCAS 85) and given in the table, which shows that an average of 28% improvement is achieved over [17]. This improvement is because of (i) heuristic based reordering algorithm and (ii) the proposed algorithm starts by test vector with minimum initial switching activity.

The results are also compared with existing meth-

ods [10, 11] and improvement in switching activity is achieved. In [11], the reordering algorithm is developed using Genetic algorithm in which the bits of test vectors are modified and the fault coverage of the CUT is reduced. But the proposed algorithm does not affect the bits and hence the fault coverage remains same. Hence the proposed algorithm is more effective in reducing switching activity during testing without modifying the fault coverage.

To understand the concept of power consumption during testing, a graph is drawn for switching activity of the circuit when test vectors are applied in specified order. This is shown in Fig. 1 for the benchmark circuit C880. The graph is drawn for switching activity of the circuit when ordered and unordered test vectors are applied. This shows that switching activity of ordered set is always lesser than that of unordered test set during entire period of testing. The average switching activity of Ordered and unordered test set is 162 and 326 respectively. Hence 50% of improvement is achieved in average switching activity over the unordered switching activity. This shows that both average and peak powers are reduced significantly when ordered test set is applied for testing.

The parameters such as Testing time, Fault coverage and Hardware overhead are not affected due to the proposed algorithm when compared with conventional testing techniques. This is explained as follows.

time depends on number of test vectors (n) of the CUT. Totally n test vectors are needed for testing with maximum fault coverage. Testing time is increased only when n is increased. But the proposed algorithm only reorders the pattern and n remains same. Hence testing time is same as in conventional methods.

coverage depends on the binary pattern of test vector. The binary pattern is also not altered in the reordering algorithm. Hence the fault coverage of the CUT is not affected due to the algorithm.

area overhead: BIST is advanced method used for periodic testing of latest VLSI circuits. Test vectors and their responses are to be loaded in BIST for testing. The hardware area required for storing is depending on number of inputs of the CUT. The algorithm does not alter the number of input. Hence area overhead is not increased due to this proposed algorithm.

Further, the parameter power dissipation and energy are reduced significantly. Since the switching activity is basic cause for power dissipation in CMOS ICs, the proposed algorithm is used to reduce the switching activity of the CUT by reordering the test vector sequences. The reordered test vector set reduces both average switching activity and total switching activity. Hence the algorithm reduces both power dissipation and total energy of the CUT.

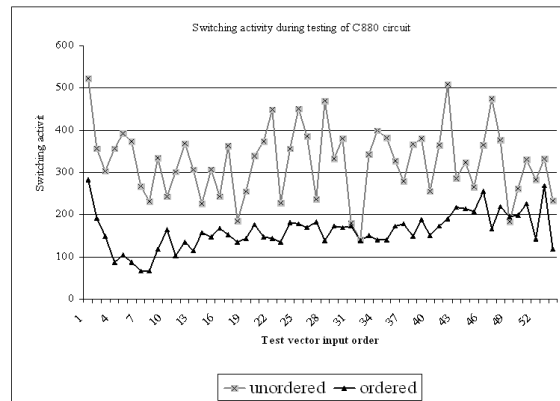
## 5. CONCLUSION

In VLSI design process, power dissipation during testing is major concern. The low power design in VLSI circuits make real needs for the test power optimization approaches of time saving and better optimization effect. A novel algorithm for the test power optimization is proposed in this paper. Since the 80% of the total power dissipation in CMOS circuits is due to the switching activity, the proposed algorithm reduces the switching activity by reordering the sequence of test vectors of the CUT. The algorithm is designed using graph theory model with heuristic approach to find more suboptimal solutions. The performance of the algorithm is tested with ISCAS85 bench mark circuits. Experimental results show that new approach reduces switching activity up to 41% when the test vectors generated by the proposed algorithm are applied during test phase. Hence there is a reduction in peak power, average power and total energy during test phase.

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**Fig.1:** Switching activity of C880 during testing



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**Table 4:** Benchmark Results of the proposed work

Ckts	FC(%)	Ckt Size (gates)	#test vector (n)	Switching activity				Percentage improvement (%imp)	swa[ ][ ] generation time(sec)
				Unordered		Ordered			
				TSA	SPT	TSA	SPT		
C17	100	6	6	52	8.7	27	4.5	48.1%	126 $\mu$ s
C432	96.98	160	36	7842	217.8	4926	136.8	37.2%	0.1
C499	100	202	100	7371	73.7	4809	48.1	34.8%	1.4
C1355	72.68	546	62	15596	251.5	7983	79.5	48.8%	1.4
C1908	99.92	880	119	7057	59.3	4391	36.9	37.8%	8.6
C6288	99.56	2416	26	186543	7174.7	127228	4893.4	31.8%	1.1
C880	100	383	54	17591	325.7	8748	162	50.3%	0.8
C2670	100	1193	202	32970	163.2	18738	92.3	43.2%	33.9
C5315	100	2307	252	85986	341.2	49012	194	43%	102.1
C3540	100	1669	154	42170	273.8	33450	217.2	20.7%	27.5
C7552	100	3512	263	146272	556.2	92151	350.7	37%	169.4
Average								39.34%	

**Table 5:** Comparison Results with previous phase of the proposed work

circuit	Total Switching Activity (TSA)		Percentage Improvement
	Proposed work	Previous phase[2]	
C17	27	49	44.9%
C432	4926	5174	4.8%
C499	4809	4373	-9.0%
C1355	7983	11944	33.3%
C1908	4391	3844	-1.2%
C6288	127228	131238	3.00%
Averagr			12.95%

**Table 6:** Comparison Results with existing methods [2, 4, 13] for total switching activity

circuits	Proposed work (TSA)	Existing method [2]		Existing method christofides [4]		Existing method Greedy [4]		Existing method[13]	
		TSA	%imp	TSA	%imp	TSA	%imp	TSA	%imp
C1355	7983	11417	30%	13949	43%	13315	40%	28511	72%
C1908	4391	21306	79.4%	25608	83%	24250	81%	38250	88.5%
C499	4809	-	-	5450	12%	4920	2%	-	-
C880	8748	6658	23.9%	8918	1.94%	8183	-6.4%	6403	-26.8%
C2670	18738	20841	10.1%	25296	35%	21917	14.5%	27921	32.9%
C5315	49012	60040	18.4%	106390	53.9%	93610	47.6%	90101	45.6%
C3540	33450	82379	59.4%	72458	53.8%	66443	49.7%	67603	50.5%
C7552	92151	121304	24.0%	163742	43.7%	142614	35.4%	159414	42.2%
Average			35.03%		40.79%		33%		43.6%

**Table 7:** Comparison Results with existing methods [2, 4,] for average switching activity

circuits	Prop. work (SPT)	Existing method [2]				Existing method christofides [4]			Existing method Greedy [4]		Test vector overhead in[4]
		SPT	Test vectors	%imp (SPT)	Test vector overhead	SPT	Test vectors	%imp (SPT)	SPT	%imp (SPT)	
C1355	79.4	82.1	139	3.2	224%	140.9	99	43.5	134.5	40.8	160%
C1908	36.9	105.9	201	65.2	169%	175.4	146	78.9	166.1	77.8	122%
C499	48.1	-	-	-	-	54.5	100	11.7	49.2	2.2	100%
C880	162	33.6	198	-79.2	366%	91	98	-43.8	83.5	-4.8	181%
C2670	92.8	45.2	461	-51.2	228%	81.6	310	-12.0	70.7	-23.8	153%
C5315	194	84.1	714	-56	283%	289	370	32.9	252.9	23.2	147%
C3540	217.2	235.4	350	-7.7	227%	319	227	32	292.7	25.7	147%
C7552	350.7	165.5	733	-52	278%	589	278	40.5	513.1	31.6	105%
Average				-23	254%			23		16.2	139%

**Table 8:** Comparison Results with existing method [17] for total switching activity

Circuits	Proposed work TSA	Existing method 2-opt [17]		Existing method webex [17]	
		TSA	%imp of proposed work	TSA	%imp of proposed work
C1355	7983	12793	37.5	12622	36.7
C1908	4391	28731	84.7	28420	84.5
C499	4809	3178	-33.9	3109	-35.3
C880	8748	5504	-37	5516	-36.9
C2670	18738	31624	40.7	31492	40.5
C5315	49012	89309	45	88840	44.8
C3540	33450	55937	40.2	55903	40
C7552	92151	19879	53.6	201741	54.3
Average			28.85		28.6