ABSTRACT

An integrable temperature compensation technique for CMOS current controlled current conveyor (CCCII) is proposed. It uses a current biasing circuit which has a current that is directly proportional to the absolute temperature and can also be electronically controlled. The HSPICE simulation results through the BSIM3v3 model parameters of 0.5 μm CMOS technology from MOSIS are given here. Furthermore, basic application examples as a current controlled second-order bandpass filter and a floating inductance simulator have been also considered.

Keywords: CCCII, Temperature compensation, CMOS

1. INTRODUCTION

Second generation current conveyor (CCII) is a versatile analog device which is used to implement many analog signal processing functions such as active filters, impedance simulators, and oscillators, etc. This current-mode device offers several advantages, such as greater linearity and wider bandwidth over voltage-mode active device likes op-amps [1]. The recently introduced second generation current controlled current conveyor (CCCII) [2-4] has the advantage of electronic adjustability over the CCII. CCCII allows the adjustment of the x-terminal intrinsic resistance via a bias current. Unfortunately, this resistance is directly proportional to thermal voltage for bipolar technology [2] and surface mobility (μ) for CMOS technology [6]. This means that the characteristics of the current controlled current conveyor-based circuits will strongly depend on the absolute temperature. Therefore, a technique of temperature compensation is required.

In bipolar technology, this problem has been solved using bias circuit, the principle is to generate a current that directly relates to the thermal voltage [5]. However, this technique cannot be used in CMOS technology.

In this paper, a temperature compensation technique for CMOS CCCII is proposed. This technique uses current biasing circuit with current directly proportional to μCox and current divider circuit to generate bias current for CCCII. The principal feature of the proposed circuit is that the circuit employs only CMOS and some external voltage and current sources such that the circuit can be easily integrated on one chip. Simulation results of the compensated CCCII by HSPICE through a 0.5μm CMOS technology are given to confirm the performance of the proposed circuit. In addition, simulation results of compensated CCCII in application examples, as a second-order bandpass filter and a floating inductance simulator are also included here.

2. CIRCUIT DESCRIPTION

2.1 Conventional CCCII

The matrix-relationship between the voltage and current variables among port X, Y and Z of an ideal CCCII can be described by the following matrix equation

\[
\begin{bmatrix}
  i_x \\
  v_x \\
  i_y \\
  v_y \\
  i_z \\
  v_z
\end{bmatrix}
= \begin{bmatrix}
  0 & 0 & 0 \\
  1 & R_x & 0 \\
  0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
  v_x \\
  i_x \\
  v_y \\
  v_z
\end{bmatrix}
\pm
\begin{bmatrix}
  v_x \\
  v_y \\
  v_z
\end{bmatrix}
\]

(1)

where the positive and negative signs of the current i_z denote the positive (CCCII+) and negative type (CCCII-), respectively, and R_x is the X-terminal intrinsic resistance of CCCII.

The circuit configuration for conventional CMOS CCCII+ is illustrated in Fig.1, which based on complementary source follower [6]. The X-input impedance is calculated as

\[ R_x \approx \frac{1}{(g_{m10} + g_{m11})} \]

(2)

where g_m denote the transconductance of transistor number i, respectively. If matched transistors are considered (M10 matching M11), that is g_{m10} = g_{m11}, then

\[ R_x = \frac{1}{\sqrt{8\beta I_0}} \]

(3)

where \( \beta = \beta_{m10} = \left( \frac{\mu C_{ox} W}{L_{M10}} \right) \) = \( \beta_{m11} = \left( \frac{\mu C_{ox} W}{L_{M11}} \right) \). Since transconductance of transistor is proportional to \( 1/\sqrt{I_0} \), so that it is possible to control its value by changing the bias current. The temperature stability of R_x strongly depends on physical parameter; \( \beta \) of the CMOS, when temperature dependence is dominated on \( \beta \) as followed [7]
Fig. 1: Conventional CMOS CCCII+

Fig. 2: Current Biasing Circuit

\[ \beta = \beta_0 \left( \frac{T}{T_0} \right)^{1.5} \]  \hspace{1cm} (4)

where \( \beta_0 \) is a reference physical parameter of the CMOS at a reference temperature; \( T_0 \). Hence, temperature coefficient of \( R_x \) can be obtained as

\[ \frac{1}{R_x} \frac{\partial R_x}{\partial T} = \frac{3}{4} T^{-1}. \]  \hspace{1cm} (5)

It can be found that, from equation (5), \( R_x \) contributes a positive temperature coefficient, thus current biasing circuit that provides a negative temperature coefficient is required for the compensation.

2.2 Proposed Technique

The principle of proposed temperature compensation technique is based on a current biasing circuit that generates a current with a negative temperature coefficient. Fig. 2 shows the current biasing circuit which generates a current that directly relates to the absolute temperature. Transistors MR1, MR2, MR8 and MR9 function as a current reference generator [8] and generate a current \( I_a \) of the form

\[ I_a = \left( \frac{\mu C_{ox}}{2} \right) \frac{W}{L} \frac{V}{1 - \sqrt{m}} \]  \hspace{1cm} (6)

where \( m = \frac{(W/L)_{MR1}}{(W/L)_{MR2}} \frac{(W/L)_{MR3}}{(W/L)_{MR9}} \) and \( 0 < m < 1 \).

To obtain low supply regulation sensitivities, cascode transistors, MR3 to MR7, are added to current mirror of circuit. The current reference \( I_a \) is available through MR12.

MR13 to MR19 function as current multiplier-divider [9] and provide an output current \( I_o \) of the form

\[ I_o = \frac{I^2_a}{I_a} = \frac{I^2_a}{(\frac{\mu C_{ox}}{2}) \frac{W}{L} \frac{V}{1 - \sqrt{m}}}. \]  \hspace{1cm} (7)

where \( I_a \) is the external bias current.

Fig. 3 shows the completed circuit schematic of temperature compensated CMOS CCCII and its transistor dimensions are listed in Table 1. Using equations (3) and (7), the intrinsic resistance \( R_x \) can be found as

\[ R_x = \frac{1}{\sqrt{8 \beta I_a}} \left( \frac{\mu C_{ox}}{2} \frac{W}{L} \frac{V}{1 - \sqrt{m}} \right). \]  \hspace{1cm} (8)

If \( \left( \frac{\mu C_{ox}}{L} \right) = \beta \), then

\[ R_x = \frac{V}{4(1 - \sqrt{m}) I_o}. \]  \hspace{1cm} (9)

Now we can see that \( R_x \) is temperature insensitive and can be controlled by \( I_o \).

Table 1: Transistor Aspect Ratio

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L (um/um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR1-MR4</td>
<td>12/2.4</td>
</tr>
<tr>
<td>MR5-MR10</td>
<td>50/5</td>
</tr>
<tr>
<td>MR11-MR12</td>
<td>50/2.4</td>
</tr>
<tr>
<td>MR13, MR14, MR15, MR16, MR19</td>
<td>5/5</td>
</tr>
<tr>
<td>MR17, MR18, MR20, MR21</td>
<td>50/5</td>
</tr>
<tr>
<td>M1, M2, M3, M5, M8, M9, M11</td>
<td>12/2.4</td>
</tr>
<tr>
<td>M4, M6, M7, M10, M12, M13</td>
<td>55/2.4</td>
</tr>
</tbody>
</table>

3. SIMULATION RESULTS

The performance of the proposed circuit in Fig. 3 was simulated using HSPICE through a MOSIS 0.5 μm CMOS process BSIM3v3 model parameters. The circuit was operated with ±3 V supply, the currents \( I_a \) is set to 85 μA, \( V = 250 \) mV and an input signal voltage is applied at port X. The simulation results are shown in Fig. 4, which displays the resistance at port X against temperature variations.
The simulation result in Fig. 4 shows that the temperature performance of the compensated circuit is much better than that of the conventional circuit. The maximum resistance deviations of conventional and compensated circuit are approximately equal to 25.24 and 3.34 %, respectively, in temperature range -20 to 100 °C.

Equation (11) indicates that the value of $\omega_0$ is adjusted by bias current of CCCII+s without affecting either the quality factor or the gain.

The filter circuit was simulated with $I_b = 80 \mu A$ and $V = 250 \text{ mV}$ for CCCII+s. The simulation results in Fig. 5 show the frequency responses obtained with $C_1 = 4 \text{nF}$ and $C_2 = 10 \text{nF}$ at temperature 0, 27 and 75 °C, compared between the conventional CMOS CCCII+ and the temperature compensated CMOS CCCII+, as depicted in Fig. 5(a) and (b), respectively.
4.2 Floating Inductance Simulation

The floating inductance simulator, which is modified from [10], employs four CCCII+s and one grounded capacitor. The equivalent impedance is given by

\[ Z_{eq} = (R_{s1} + R_{s2})(R_{s3} + R_{s4})C \sin s \]  

(13)

When all bias currents are identical, the equivalent inductance is

\[ L = 4R^2C = \frac{1}{4} \left( \frac{V}{1 - \sqrt{m}} \right)^2 I_b \]  

(14)

From Equation (14), it can be found that the inductance can be controlled by the bias current.

The performance of inductance simulator was verified by series RLC resonance circuit with R = 1kΩ and C = 1nF. The current characteristics of the circuit are shown in Fig. 6 with different temperatures as 0, 27 and 70 °C.

5. CONCLUSION

In this paper, a temperature compensation technique for CMOS CCCII has been proposed. A current biasing circuit with a current proportional to absolute temperature is used to compensate the temperature sensitivity of a CMOS CCCII. The simulation results obtained from HSPICE confirm that the temperature compensated circuit is less temperature sensitive than conventional circuit, the simulation results of application examples as second-order bandpass filter and inductance simulator are additionally good evidences. Also, the resulting circuit is suitable for further implementing in integrated circuit.

6. ACKNOWLEDGEMENT

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7. REFERENCES