Abstract- This paper describes a multiphase sinusoidal oscillator based on the use of Current Differencing Buffered Amplifiers (CDBAs). The proposed oscillator provides output signals both in voltage and current forms simultaneously. It comprises $N$ cascaded lossy integrators and an inverter, and generates $N+1$ sinusoidal signals with $180^\circ/N$ phase difference. The SPICE simulation results obtained using AD844 macro model are given to confirm the theoretical analysis.

I. INTRODUCTION

The wide use of the multiphase sinusoidal oscillators (MSOs) in power controllers, communication system and signal processing [1-5] have stimulated the development of the MSOs. Voltage-mode operational amplifiers (op-amps) are widely used for realizing the multiphase sinusoidal waveforms [6] due to their commercial availability. However, circuit synthesis techniques in current domain using current conveyors [7], current followers [8] and operational transductance amplifiers [9] have gained substantial interests. The main advantages of processing signal in current form are wide bandwidth, high slew rate and independent gain realization without a constant gain-bandwidth product constraint.

Recently, a new active building block named as a current differencing buffered amplifier (CDBA) has been introduced [10]. Since the CDBA consists of a unity-gain differential amplifier and a unity-gain voltage amplifier, a high frequency operation and less parasitic can be expected. The MSO based on CDBAs has been reported in the literature [11], however it can produce only sinusoidal voltage output. This paper presents a CDBAs based MSO circuit, which is possible to provide output sinusoidal signals in both voltage and current forms simultaneously. The oscillator structure is constructed by cascading of $N$ stages current domain lossy integrators and a current inverter. Consequently, the $N+1$ outputs with $180^\circ/N$ phase difference are available.

II. CIRCUIT DESCRIPTION

The circuit symbol of the CDBA is shown in Fig. 1, where $p$ and $n$ are the input terminals, $z$ and $w$ are the output terminals. Its current and voltage characteristics can be described by the following relations [1-2]

$$v_p = 0, \quad v_n = 0, \quad i_z = i_p - i_n \quad \text{and} \quad v_w = v_z.$$  

According to Eq. (1), an output current at the $z$-terminal $i_z$ follows the difference of input currents through the $p$-terminal and $n$-terminal. Then, the output current is converted into an output voltage $v_w$ through an impedance connected at the terminal $z$. Although there are numerous techniques to realize the CDBAs, a popular one is obtained by using two commercially available CFOAs, AD844 [12], as shown in Fig. 2 [13]. Fig. 3 shows a general block diagram of the MSO for $N+1$ phase sinusoidal oscillator. It is constructed by cascading $N$ stages of current domain lossy integrators and a current inverter. The output current $I_{o,N}$ of the last stage is fed back to the first stage through the current inverter. Therefore, the transfer function between $I_i$ and $I_{o,N}$ can be written as:

$$\frac{I_{o,N}}{I_i} = \left( \frac{K}{1+Ts} \right)^N = -1,$$  

where $K$ is DC current gain of each stage and system time constant ($T$) is $1/\omega_c$, when $\omega_c$ is the internal-pole of the lossy integrator. By expanding Eq. (2), the characteristic equation is obtained as

$$(1+Ts)^N + (-1)^{N+1} K^N = 0.$$  

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By replacing \( s = j\omega_0 \), into Eq. (3), we can find the oscillation frequency and oscillation condition. It can be proved that this equation will give a realistic solution only for \( N \geq 3 \). To solve for \( K \) and \( \omega_0 \), the real and imaginary parts of Eq. (3) are set to zero. In case of \( N = 3 \), Eq. (3) yields

\[
(1 + j\omega_0 T)^3 + K^3 = 0 ,
\]

hence,

\[
1 - 3\omega_0^2 T^2 + K^3 = 0 ,
\]

and

\[
3j\omega_0 T - j\omega_0 T^3 = 0
\]

where \( \omega_0 \) is the oscillation angular frequency. The oscillation frequency \( f_0 \) of this case is obtained by solving equation (6) as

\[
f_0 = \frac{\sqrt{3}}{2\pi T} .
\]  

Substituting Eq. (7) into (5) will give the oscillation condition that is \( K = 2 \). The conditions of the MSO for the others \( N \) can be obtained in a similar way and will result in the MSO with \( N + 1 \) outputs. Each output is equal in amplitude and has phase shift by \( 180^\circ /N \).

III. PROPOSED CDBA-BASE MULTIPHASE SINUSOIDAL OSCILLATOR

According to the block diagram representation of the MSO shown in Fig. 3, the system consists of two repeated sub-blocks: current domain lossy integrator and current inverter. In this work, two new sub-blocks using the CDBA are introduced in Fig. 4. To perform lossy integrator function, the proposed sub-block consisting of one CDBA, three resistors and one capacitor is shown in Fig. 4(a). The current transfer function \( I_o/I_i \) can be written as

For simplicity sake, the current inverter is designed using the CDBA as shown in figure 4(b). From Eq. (1), when the input current at terminal \( p \) is absent, the current transfer function \( (I_o/I_i) \) is obtained equal -1.

By substituting our proposed sub-circuits into the general block diagram of the MSO in Fig. 3, the complete circuit of the CDBA-based MSO for \( N = 3 \), which has 60° phase difference, can be obtained as shown in Fig. 5. Since our proposed structure exploits an advantage of having both voltage and current outputs of the CDBA, the resulting MSO will be able to produce the sinusoidal signals in voltage and current forms simultaneously. This gives a potential to apply this circuit in wider range of applications. The current and voltage transfer function between each lossy integrator stage are equivalent and can be directly represented use by Eq. (8). For the sake of
design, let us select the circuit components such that \( R_1 = R_3 \).

Therefore, the current and voltage transfer function are

\[
\frac{I_{o,N}}{I_{o,N-1}} = \frac{V_{o,N}}{V_{o,N-1}} = \frac{K}{1 + Ts} = \frac{(R_2/R_3)}{1 + sCR_2}
\]

(9)

The oscillation conditions and the oscillation frequency solving from Eq. (4) of this circuit are

\[
K = \frac{R_2}{R_3},
\]

(10)

\[
f_o = \frac{\sqrt{3}}{2\pi R_2 C}
\]

(11)

As already determined in the previous section, the oscillation condition is satisfied when \( K = 2 \) or \( R_2 = 2R_3 \). It should be noted that, the output voltages are ready to be used since they appear at the voltage output ports of the CDBAs. However, the current outputs need additional ports to duplicate the desired signals to the next stage. This configuration is easily implemented by employing multi-output current mirrors in many customed design CDBAs available both Bipolar and CMOS technology [14 -15].

IV. SIMULATION RESULTS

Simulation results of the proposed circuit as depicted in Fig. 5 are obtained using the PSPICE circuit simulator with ±18V supply voltage. To verify the proposed circuit, the dual-mode MSO is designed at 27.6 kHz oscillation frequency. Hence, the capacitor and resistors are calculated by using Eq. (10) and (11), that are \( C = 1 \mu F, R_1 = R_3 = 5 \, \text{k}\Omega \) and \( R_2 = 10 \, \text{k}\Omega \). The CDBA was constructed using two AD844 as shown in Fig. 2. In fact, there are non-zero impedances at the input ports, \( p \) and \( n \), that cause the current transfer error and hence resulting in an oscillation condition violation (\( K < 2 \)). In order to compensate this error, the resistor \( R_1 \) and \( R_3 \) have to be reduced to satisfy the oscillation condition (\( K > 2 \)). In this case, \( R_1 = R_3 = 4.7 \, \text{k}\Omega \) is selected and \( K = 2.087 \) is obtained. The simulated oscillation frequency of 28 kHz is

![Figure 5](image-url)

The proposed CDBAs-base multiphase sinusoidal oscillator, which can generate 4 outputs current and 4 outputs voltage different phase sinusoidal both voltage and current signal output each shifted in phase by 60°.

![Figure 6](image-url)

The simulated output voltage \( (V_{o,0}, V_{o,1}, V_{o,2}, V_{o,3}) \) and output current \( (I_{o,0}, I_{o,1}, I_{o,2}, I_{o,3}) \) over time at frequency of 28kHz.

![Figure 7](image-url)

Frequency spectrum of the waveform in Fig. 6.
observed and its output voltages \((V_{o,0}, V_{o,1}, V_{o,2}, V_{o,3})\) and output currents \((I_{o,0}, I_{o,1}, I_{o,2}, I_{o,3})\) over time are shown in Fig. 6. The outputs have equal amplitude of 13.3 V and 2.83 mA for voltage and current signals, respectively. Fig. 7 shows frequency spectrum of the output current signal, which has the total harmonic distortion (THD) about 1.19 %. Note that the oscillation frequency is slightly higher than the calculation. This can be explained by considering Eq. (5). It can be seen that increasing \(K\) will also make \(o_0\) higher.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Oscillation frequency</th>
<th>Phase comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>(C = 0.1 \text{ nF})</td>
<td>(f_e = 276 \text{ kHz})</td>
<td>(I_{o,0} - I_{o,1})</td>
</tr>
<tr>
<td>(C = 1 \text{ nF})</td>
<td>(f_e = 27.6 \text{ kHz})</td>
<td>(28 \text{ kHz})</td>
</tr>
<tr>
<td>(C = 10 \text{ nF})</td>
<td>(f_e = 2.76 \text{ kHz})</td>
<td>(2.8 \text{ kHz})</td>
</tr>
<tr>
<td>(C = 0.1 \text{ µF})</td>
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</table>

The simulation results when varying the capacitor \(C\) to 0.1 nF, 1 nF, 10 nF, 0.1 µF and 1 µF, are summarizable in TABLE I. The expected oscillation frequency, the simulated oscillation frequency and the phase difference of the output currents \((I_{o,0}, I_{o,1}, I_{o,2}, I_{o,3})\) with respect to \(I_{o,0}\) are given. For the frequency of 28 kHz and lower, the frequency error and phase shift error of less than 1.82 % and 1.7 % are observed, respectively. These errors are larger at higher frequency due to the limitation of the employed AD844. Therefore, for the high frequency applications, a high performance CDBA's either implemented in CMOS or Bipolar technology should be properly designed to overcome this problem. Fig. 8 shows simulation results of the MSOs for \(N = 4\) at frequency 28 kHz.

The output voltage \((V_{o,0}, V_{o,1}, V_{o,2}, V_{o,3})\) and output current \((I_{o,0}, I_{o,1}, I_{o,2}, I_{o,3})\) have equal amplitude of 13.3 V and 3.5 mA, respectively.

V. CONCLUSION

A new multiphase sinusoidal oscillator based on CDBAs is proposed. The proposed circuit can generate sinusoidal waveforms of both voltage and current signals in the same circuit, so it can be applied in both voltage mode and current mode applications. The circuit can realize \(N+1\) difference phase sinusoidal output signals by using \(N\) cascaded lossy integrators and an inverter. This circuit possesses another advantage of that the oscillation condition can be always realized from resistor ratio for every chosen oscillation frequency. The simulation results confirm the theoretical conclusions very well.

REFERENCES

A. An Electronically and linearly tunable CMOS OTA (EOTA)

Figure 1 shows a balanced single-output CMOS OTA, which is formed by MOS coupled pair and current mirrors, where $V_{in}$ is the differential input voltage ($V_{in} = V_1 - V_2$), $i_o$ is the output current and $I_{BB}$ is the bias current. Let us assume that $M_1$ and $M_2$ are perfectly matched and the current mirrors have unity current gain. By using equation (1), the differential output current of the circuit in Figure 1 can be given by

$$i_o = g_m V_{in}$$

(2)

The transconductance gain ($g_m$) of the MOS coupled pair can be derived by taking the derivative of (2) with respect to $V_{in}$, yielding

$$g_m = \frac{d}{dV_{in}} i_o = \frac{\sqrt{2} I_{bb} K}{2 I_{bb}} , \text{ for } \frac{I_{bb}}{K} \leq V_{in} \leq \sqrt{\frac{I_{bb}}{K}}$$

(3)

A CMOS-based electronically and linearly tunable OTA, called as an EOTA [10], that realized by using three OTAs the circuit diagram shown in figure 1.

B. The proposed electronically and linearly tunable sinusoidal quadrature oscillator

The proposed electronically tunable sinusoidal quadrature oscillator is constructed by using EOTAs and OTAs
Figure 5. Frequency tunable range of the oscillator

Figure 5 demonstrates the oscillation frequency that can be tuned with respect to the dc bias-current $I_{BE1}=I_{BE2}=I_{BE}$, where the bias current is varied from 100μA to 1000μA. The figure shows that, for the cases of $C=20nF$, $C=10nF$ and $C=1nF$, the oscillation frequency ranges are in the frequency ranges of 500 Hz to 5 kHz, 1 kHz to 10 kHz and 10 kHz to 98 kHz, respectively, with the error of less than 5%. This result demonstrates that the maximum frequencies up to 98 kHz is achieved by reducing the capacitance values ($C_1=C_2=C=1nF$).

IV. CONCLUSIONS

A design of CMOS-based electronically tunable quadrature oscillator has been proposed. The oscillator is realize by using two EOTAs, two OTAs and two grounded capacitors which is suitable for implementing in CMOS integrated form. Its oscillation frequency can be electronically and linearly tuned for a wide range by the transconductance gain without affecting the oscillation condition and the capability of operation at high frequencies. Simulation results have been employed to demonstrate the performances of the proposed oscillator.

REFERENCES

The $g_m$-C quadrature oscillator based on the use of EOTAs is shown in Fig. 3. The quadrature oscillator circuit diagram is similar to the bipolar-based quadrature oscillator circuit of the reference 11. The basic building blocks of the oscillators consist of two integrators cascaded in a loop; an inverting integrator (EOTA and $C_1$) and a non-inverting integrator (EOTA$_2$ and $C_2$). It should be noted that a regenerative circuit made by the balance CMOS OTA, OTA$_3$ and OTA$_4$, are included in order to place the poles in the right-half complex plane so that the circuit is unstable and self-starting, from equation (7), the characteristic equation of the oscillator can be express as

$$s^2 - s \left( \frac{g_{m3} - g_{m4}}{C_1} \right) + \frac{g_{m1}g_{m2}}{C_1C_2} = 0$$  \hspace{1cm} (9)$$

Therefore, in order to initially locate the poles inside the right-half complex frequency plane to assure self-starting operation, the condition for the oscillation can be start as

$$g_{m3} - g_{m4} \geq \varepsilon$$  \hspace{1cm} (10)$$

or

$$\sqrt{I_{BE3}} - \sqrt{I_{BE4}} \geq \varepsilon$$  \hspace{1cm} (11)$$

where $\varepsilon$ is a small positive number. The oscillating frequency is

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$$  \hspace{1cm} (12)$$

It is obvious from (12) and (13) that the oscillation frequency can be tuned without disturbing the oscillation. Moreover, the frequency of oscillation $\omega_o$ can be linearly controlled by adjust the dc bias current $I_{BE1}=I_{BE2}=I_{BE}$.

**III. SIMULATION RESULTS**

The performance of the proposed electronically and linearly tunable sinusoidal quadrature oscillator of figure 3 was verified through the use of PSPICE simulation results. All the balanced CMOS OTA and EOTAs were simulated by using CMOS transistor parameters of the SCN2 level 2 of MOSIS [12]. The dimensions of transistors $M_1$ and $M_2$ are $W=50\mu m$ and $L=10\mu m$. The dimensions of the transistor $M_3-M_8$ are $W=100\mu m$ and $L=10\mu m$. The power supply voltage were set to $V_{DD}=-V_{SS}=\pm 5V$.

Figure 4 shows the results obtained from the electronically and linearly tunable quadrature oscillator circuit of figure 3 in the case of $C_1=C_2=C=20nF$, $I_{BE1}=I_{BE2}=I_{BE}=1mA$, $I_{BE3}=I_{BE4}=1mA$, $I_{BE}=0.995\mu A$, with $\varepsilon = \sqrt{2I_{BE3}K_3} - \sqrt{2I_{BE4}K_4} = 1.26\mu A$. The simulated oscillation frequency with quadrature outputs of equal magnitude of about $5kHz$ is achieved. The circuit provides the oscillation frequency with the error of less than 5%, since the predicted oscillation frequency from the equation (13) is about $4.8kHz$.

![Figure 4](image-url)