Devices Design, Fabrication and Characterizations of 0.8 µm CMOS Technology

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Abstract-This paper describes the concept, design and characterizations of 0.8 CMOS for technology development at Thai MicroElectronics Center (TMEC). Both NMOS and PMOS have been designed form concept and using the process simulation software TSUPREM-4 and device simulation software MEDICI. Device design emphasis for example threshold voltage, off state leakage current, punctthrough voltage and Drain Induced Barrier Lowering (DIBL) effect have been seriously investigation to improve the device performance. Furthermore, the sensitivity of following parameters such as N-well dose and energy, voltage threshold adjust (VTA) dose and energy, gate oxide thickness and gate length variation have been determined. Extraction of devices model have been done on test chip. Based on measurements results, the I-V characteristics of MOSFET and Voltage Transfer Characteristics (VTC) of a testing inverter were present.

I. INTRODUCTION

TMEC have been developed the 0.8 µm CMOS technology fabrication. Some parameters such as threshold voltage, off state leakage current, punchthrough voltage, and subthreshold behaviors should be carried out and determined. TSUPREM-4 and MEDICI are used to simulate that act as a guide line. In this paper, the design, fabrication and device characterization of 0.8 CMOS technology were proposed

II. DEVICE DESIGN

Twin well process is used for NMOS and PMOS independently. The N-well and the P-well were fabricated by phosphorus with dose of 3.6×10¹² cm⁻² and boron implantation with dose of 6×10¹⁶ cm⁻². For its dose, N-well and P-well doping concentration were approximately 3.0×10¹⁶ cm⁻³ and 1.0×10¹⁶ respectively. Both well are done on p type substrate 5 ohm-cm of resistance. In order to minimize the complexity of fabrication process, n⁺ polysilicon is fabricated for gate electrode. A boron ion implantation for threshold voltages adjust in a channel was implemented in order to match the threshold voltage of the NMOS and PMOS device, as require in the modern CMOS technology process. As a result, a surface channel and a buried channel are formed in NMOS and PMOS respectively. The magnitudes of threshold voltage depend on various parameters in channel doping implants simulated by MEDICI shown in Fig.1. In order to get the threshold voltage [V_TH]=1.0 V for NMOS and PMOS, the N-well implantation dose must be 4.5×10¹² cm⁻² and the boron implantation dose must be more than 9.0×10¹¹ cm⁻². Fig.2 shown the threshold voltage of both MOSFET versus gate length and oxide thickness also. The threshold voltage is change rapidly as the gate length is less than 0.6 µm. The low threshold voltage is designed to improve the output current. The Anti-punchthrough implantation of NMOS is used for punchthrough suppression. The energy is 50 KeV. So that the channel peak concentration is approximately the S/D junction depth to reduce the lateral widening of depletion region at the drain end and prevents the Drain Induced Barrier Lowering (DIBL) effect also.

For isolation, the field oxide thickness is 650 nm. The field threshold voltage which is more than 15 V for supply operation under the thick field oxide is designed. The N-field implantation beneath the field oxide is implanted for increasing the field threshold voltage. However, the bird’s break encroachment must be controlled in order to affect the source/drain formation. Besides this effect, the bird’s break encroachment into the active area must be determined in order to know the minimum design gate width which has an
enough active area will be form. To reduce the hot carrier, phosphorus with $6 \times 10^{12}$ cm$^{-2}$ and boron with $1 \times 10^{13}$ cm$^{-2}$ is implemented to form the lightly doped drain (LDD) of NMOS and PMOS structure. As and BF$_2$ are implemented to produce source/drain to achieve 54 $\Omega$/sq for n$^+$ and 65 $\Omega$/sq for p$^+$ source/drain. From simulation results, the S/D junction depth was 0.3 and 0.5 $\mu$m for NMOS and PMOS and the effective channel length was approximately 0.6 $\mu$m of both MOSFET also. The shallow junction will be improved the subthreshold swing to 80 mV/dec and minimized the Drain Induced Barrier Lowering(DIBL) effect.

### III. Process Fabrication

Twin well process are fabricated for NMOS and PMOS independently. The N-well and the P-well were implemented by phosphorus with dose of $3.6 \times 10^{12}$ cm$^{-2}$ and boron implantation with dose of $6 \times 10^{11}$ cm$^{-2}$. For its dose, N-well and P-well doping concentration were approximately $3.0 \times 10^{16}$ and $1.0 \times 10^{17}$ cm$^{-3}$ respectively. Both tubs are done on p type substrate 5 ohm-cm. In order to minimize the complexity of fabrication process, n$^+$ polysilicon is fabricated for gate electrode. A self align n$^+$ polysilicon gate was 350 nm in thickness and gate oxide was 25 nm in thickness. A boron ion implantation for threshold voltage adjusts in a channel was implemented in order to match the threshold voltage of the NMOS and PMOS device, as require in the modern CMOS technology process. As and BF$_2$ are implemented to produce source/drain to achieve 54 $\Omega$/sq for n$^+$ and 65 $\Omega$/sq for p$^+$ source/drain. The 350 nm polysilicon is grown on gate oxide and used phosphorus implantation to form n$^+$ polysilicon gate. After NMOS and PMOS LDD implantation, the sidewall is formed and the following S/D implantations are done. The annealing process 900$^\circ$C, 30 min is done to activate impurity and maintain the impurity doping profile. After front end process, the oxide, SOG and oxide dielectric layer is deposited and reflow at 750$^\circ$C. The contact windows are opened and 30/80 of Ti/TiN are deposited and follow by metal1,TiN deposition and patterning. After an IMD layer is deposited follow by the via, windows are opened. The metal 2 and TiN are deposited and patterned. The next deposition layer is nitride to act as a passivation layer. After passivation layer, the pad window is opened to measure.

### IV. Device Characterization

Measurement and extraction of a testing device are tested on a test chip. Some performance such as threshold voltage, saturation drain current, leakage current and punchthrough voltage have been determined. All I-V characteristics measurements have been done at the room temperature. The measurement system is consisted of probe station cascade ALESSI REL6100 model, semiconductor parameter analyzer HP4156B, Precision LCR meter HP 4184A, low leakage switch E5250A and ICS software for measurement through PC computer as a controller. The device parameters with N-well dose of $3.6 \times 10^{12}$ cm$^{-2}$ and VTA with dose of $9 \times 10^{11}$ cm$^{-2}$ are illustrated in table I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NMOS</th>
<th>PMOS</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold Voltage</td>
<td>0.77</td>
<td>-0.68</td>
<td>V</td>
</tr>
<tr>
<td>Body Factor</td>
<td>0.6</td>
<td>0.64</td>
<td>V$^{-1}$</td>
</tr>
<tr>
<td>Process Transconductance</td>
<td>74.6</td>
<td>26.3</td>
<td>$\mu$A/V$^2$</td>
</tr>
<tr>
<td>Effective Channel Length</td>
<td>0.57</td>
<td>0.78</td>
<td>$\mu$m</td>
</tr>
<tr>
<td>Width Encroachment</td>
<td>0.18</td>
<td>0.2</td>
<td>$\mu$m</td>
</tr>
<tr>
<td>Punch Through Voltage</td>
<td>12</td>
<td>-13</td>
<td>V</td>
</tr>
<tr>
<td>Leakage Current</td>
<td>1</td>
<td>1.5</td>
<td>$p$A/µm</td>
</tr>
<tr>
<td>Maximum Drain Current</td>
<td>328</td>
<td>148</td>
<td>$\mu$A/µm</td>
</tr>
<tr>
<td>Poly Field Threshold</td>
<td>10</td>
<td>-12</td>
<td>V</td>
</tr>
</tbody>
</table>

Fig.3 shows the $I_{DS}$ & $V_{DS}$ of NMOS with different $V_{GS}$ (0$\rightarrow$5 V, 1V./step)

Fig.4 shows the Measured Log $I_{DS}$ & $V_{DS}$ characteristics of NMOS. The saturation current per width of NMOS and PMOS is 328 and 148 $\mu$A/µm respectively. Fig.4 shows the $I_{DS}$ & $V_{GS}$ characteristics of NMOS as the gate voltage $V_{GS}$ is sweep from 0V to 1.5 V at different drain voltage $V_{DS}$ and grounded
source and substrate together. The off stage current is in order of pA/μm for both.

The subthreshold swing is measured and compared with simulation results. The measured subthreshold swing is approximately 100mV/dec for both. The measured curve indicated that there was no punchthrough effected on a testing device same as the simulation results. The punchthrough effect is measured on I_DS &V_DS curve by sweep the drain voltage from 0 V to 20 V and ground gate and source terminal. The punchthrough voltage detected at drain current of 1nA/μm [1] is 12 V for NMOS and -13 V for PMOS.

The DIBL effect is observed by a shift of threshold voltage as a function of drain voltage. The threshold voltage measurement for testing device is performed by measuring a set of I_DS & V_DS with increasing V_DS value as a parameter. The gate voltage at which the drain current of 0.1μA/μm is claim the threshold voltage. The measured DIBL is 40mV/V and 50 mV/V of NMOS and PMOS respectively. Since the buried channel PMOS, then more leakage current flow.

Based on the spice model level 3, the extraction model parameter was done on the testing device with the W/L ratio 40/40, 40/0.8 and 0.8/40 of value. Fig.5 show the measurement and simulation I-V curve for 40/0.8 NMOS device. It can be seen that the prediction model does not fit well with experiment. This may be because of limitations in spice model level 3.

For a basic circuit testing, we test the basic CMOS inverter with a difference size of PMOS to compare with NMOS. The minimum dimension W/L of NMOS is designed at 1.6/0.8. The Voltage Transfer Characteristics (VTC) of a testing CMOS inverter show in Fig.6. The supply drain current I_DDM versus input voltage Vin for CMOS inverter show in Fig.7. The maximum supply drain current is 130 μA at the midway of input voltage and the maximum power dissipation is a function of supply voltage.

**V. CONCLUSION**

The 0.8 CMOS technology fabrication have been designed and developed at Thai Micro Electronics Center. A single Voltage Threshold Adjust (VTA), Anti Punthrough (APT) process and n+ polysilicon gate electrode are fabricated to minimize the complexity of fabrication process can be achieved. The I-V curve show that the MOSFET is a good turn off rate in subthreshold region and no punchthrough problems. Surface DIBL investigation shows no surface leakage current. Using an inverter for a basic circuit testing, The VTC shows a good curve at Kr = 1.0.

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**REFERENCES**


