Macro-model Based SPICE Simulation of DC/DC Switching Regulators

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ABSTRACT

A macro-model is a simplified model that emulates functional characteristics of a device or circuit, and widely used in system-level simulation. In this paper, macro-model based SPICE simulation of DC/DC switching regulators is presented. Macro-models of a power switch and Pulse Width Modulation (PWM) control circuit are described. Two simulation examples are given to demonstrate the capability of these macro-models in simulating switching regulator performances.

Keywords: DC/DC switching regulators, Simulation

1. INTRODUCTION

Computer simulation plays an important role in modern design of DC/DC switching regulators. It allows a regulator’s performance to be evaluated prior to construction of a prototype; hence design flaws, if any, can be detected and corrected at the early stages in the design process, reducing time-to-market and saving costs. The switching regulator performance can be simulated on an average or a cycle-by-cycle basis [1]. Though the average simulation is known to be faster, the advantage of the cycle-by-cycle simulation nevertheless is that it yields the simulated waveforms contain a switching ripple, resembling to those found in the real converter. The ability to predict the switching ripple and ringing of the output voltage is crucial in design of power supplies for modern high speed data processing loads (e.g. microprocessors), which demand tight voltage tolerance from the power supplies [2].

Simulation time of the cycle-by-cycle simulation can be reduced considerably by using a macro-model of a device or circuit, instead of the detailed one. The macro-model is a simple model that emulates functional characteristics of a device or circuit [3]; other secondary effects are often ignored. It is widely used in system-level simulation to evaluate overall system performances. In the case of switching regulators, the macro-model can effectively simulate both steady state performance such as an output voltage and inductor current ripples, and transient performance such as an output voltage transient response due to an input voltage and/or output current change. These simulations provide an efficient mean to check a primary design without having to resort to breadboarding the circuit. Only until simulation shows a satisfactory result, the designer then can move on to build a prototype with confidence that no major design error has been overlooked. In this paper, macro-model-based SPICE simulation of a DC/DC switching regulator is presented.

2. MACRO-MODEL BASED SIMULATION

A buck switching regulator is shown in Fig. 1. The power MOSFET and diode conduct alternately, converting the DC input voltage, \( V_s \), into the lower DC output voltage, \( V_o \). There are two operating modes concerning the inductor current, \( i_L \). It could be continuous at all time, namely Continuous Conduction Mode (CCM), or fallen to zero at some points in a switching cycle, namely Discontinuous Conduction Mode (DCM). \( V_o \) is regulated by controlling the duty cycle of the power MOSFET. A control circuit consists of an error amplifier and voltage comparator. The error amplifier amplifies the difference between a reference voltage, \( V_{ref} \), and a sensed output voltage, \( V_o \). The resulting control voltage, \( V_c \), is then compared with a fixed frequency sawtooth voltage, \( V_{saw} \), generating a pulse-width modulated voltage, \( V_d \), to drive the power MOSFET to maintain the constant output voltage.

In macro-model based SPICE simulation, the power MOSFET, error amplifier, and voltage comparator in Fig. 1 will be replaced by their respective macro-models described below, and the diode by its ideal model readily available in SPICE.

2.1 Macro-model of a power MOSFET

The power MOSFET is emulated by an on/off switch, which has a macro-model shown in Fig. 2 [4]. The resistance across terminals A-B is switched between zero and high-value controlled by an external voltage at node C.
This can be explained as follows. The equivalent current flowing through terminal A-B is

\[ I_{eq} = \frac{V_i}{R_d} = \frac{V - E_g}{R_d} \]  

(1)

By assigning the controlled source \( E_1 \) equal to \( V_1 \), the equivalent voltage at terminal A-B is

\[ V_{eq} = E_g. \]  

(2)

From equations (1) and (2), the equivalent resistance across terminal A-B equals

\[ R_{eq} = \frac{V_{eq}}{I_{eq}} = \frac{E_g R_d}{V - E_g}. \]  

(3)

Letting the controlled source \( E_g \) be equal to \( V(1-V_in) \), \( R_{eq} \) becomes

\[ R_{eq} = \frac{(1-V_in) R_d}{V_in}. \]  

(4)

It can be seen from equation (4) that when \( V_{in} \) is a unit pulse signal, \( R_{eq} \) is switched between zero and a very high value. In the simulation, \( V_{in} \) is taken from the output of a voltage comparator described in Section 2.3.

2.2 Macro-model of an error amplifier

A macro-model of the error amplifier is shown in Fig. 3(a). The current source \( G_e \), which is controlled by the voltage difference between a reference voltage, \( V_{ref} \), and a sensed output voltage, \( V_o' \), together with \( R_e \) define the error amplifier function

\[ V_c = R_e (V_{ref} - V_o') \]  

(5)

where \( R_e \) is the error amplifier’s open-loop gain. The error amplifier’s cut-off frequency is determined from the values of \( C_e \) and \( R_e \)

\[ f_c = \frac{1}{2\pi R_e C_e}. \]  

(6)

An excursion of the control voltage, \( V_c \), is limited to between \( V_{c_{max}} \) and \( V_{c_{min}} \) by a voltage clamp circuit consisting of \( D_1, D_2, V_{c_{min}}, \) and \( V_{c_{max}} \).
5 and 6 respectively. The error amplifier is accessible at pins 1 (an inverting input), 2 (a non-inverting input), and 3 (an output). The feedback compensation circuit, consisting of R₁, R₂, R₃, C₁, and C₂, connected around the error amplifier helps stabilize and enhance output performance of the regulator. The PWM output signal is available at pin 11 of the IC, which drives the power MOSFET through a standard drive circuit. The pulse transformer is incorporated into the drive circuit to isolate the MOSFET’s source pin from the power circuit’s ground.

Fig. 4(b) shows a schematic macro-model of the system in Fig. 4(a). The error amplifier inside UC3825 has an open-loop gain of about 95dB and a cut-off frequency of about 90Hz. From these values, Rₑ and Cₑ of the macro-model in Fig. 3(a) are found to be 56kΩ and 30nF respectively. The regulator model in Fig. 4(b) is simulated by SPICE, running on a Pentium III, Personal Computer (PC). Fig. 5 shows simulated waveforms of Vo and iₗ from start to 2ms, for Vₛ = 22V and Rₒ = 2.5Ω. The simulation time taken is about 1.3s. It can be seen that Vo and iₗ reach the steady state values of 5V and 2A respectively after approximately 0.8ms. The short interval, where iₗ became discontinuous, can also be noticed in the figure. Fig. 6 depicts the magnified steady-state portion of the waveforms in Fig. 5. The output voltage ripple (ΔVₒ) and inductor current ripple (Δiₗ) are less than 0.1V and 1A respectively. These results agree with the experimental results measured from the prototype regulator shown in Fig. 7. Compared with their experimental counterparts, the simulated results are noise-free because parasitics in the regulator’s power circuit, which is responsible for switching noises, have not been modeled.

Fig. 5: Simulated waveforms of Vₒ and iₗ from the model in Fig. 4(b)

Fig. 6: Simulated steady-state waveforms of Vₒ and iₗ

Fig. 7: Experimental steady-state waveforms of Vₒ (top trace: 200mV/div) and iₗ (bottom trace: 1A/div)
3.2 Simulation of a power supply module for Intel Pentium processors

A power supply module for Intel Pentium microprocessors [2] is shown in Fig. 8. It is a buck regulator that converts a 5V input voltage from the front-end converter to a 1.8V output voltage supplying the processor. The regulator operates at a switching frequency of 300kHz and is capable of delivering an output current up to 20A. Linterc is an inductance of a track connecting the converter’s output to the processor’s power supply input. Cdecoup is a decoupling capacitor inserted across the Vcc and GND pins of the processor to reduce an output voltage ringing due to Linterc during transient. The processor's supply voltage (VL) is tightly regulated within ±5% of the nominal value, or between +1.89V and 1.71V, throughout the operating current (IL) range. The error amplifier is compensated to yield a system crossover frequency of 30kHz.

Fig. 9 shows a transient waveform of VL, when the processor draws a step current of 15A (i.e. from 5A to 20A), simulated by SPICE, using the presented macro-models. The simulation time is about 5.5s. It can be seen that VL is maintained well within the regulation band. The output voltage spike and ringing caused by Linterc can still be noticed, though its severity has been less by Cdecoup. This result is in close agreement with that presented in [2].

4. CONCLUSIONS

As the electronic equipment becomes more sophisticated with a trend toward operating at lower supply voltages and higher clock speeds, designing a power supply for these modern loads poses many challenges to a power supply designer. Simulation is an indispensable tool in the modern days of power supply design; it can be used to check the validity of the resulting design and the regulator’s performance under various operating conditions as well as under the influence of circuit parasitics. Adoption of simulation into the design process often results in the increased productivity and the reduced time-to-market. In this paper, SPICE simulation of DC/DC switching power supplies based on macro-models has been studied. Its potential as an efficient tool in modern power supply design has been demonstrated through the simulation examples.

5. REFERENCES